

University of Nebraska - Lincoln

DigitalCommons@University of Nebraska - Lincoln

---

Theses, Dissertations, and Student Research:  
Department of Physics and Astronomy

Physics and Astronomy, Department of

---

December 2007

# Characterization of Metalferroelectric-Insulator-Semiconductor Structures Based on Ferroelectric Langmuir-Blodgett Polyvinylidene Fluoride Copolymer Films for Nondestructive Random Access Memory Applications

Timothy J. Reece

University of Nebraska-Lincoln, reecetj@unk.edu

Follow this and additional works at: <https://digitalcommons.unl.edu/physicsdiss>



Part of the [Physics Commons](#)

---

Reece, Timothy J., "Characterization of Metalferroelectric-Insulator-Semiconductor Structures Based on Ferroelectric Langmuir-Blodgett Polyvinylidene Fluoride Copolymer Films for Nondestructive Random Access Memory Applications" (2007). *Theses, Dissertations, and Student Research: Department of Physics and Astronomy*. 3.  
<https://digitalcommons.unl.edu/physicsdiss/3>

This Article is brought to you for free and open access by the Physics and Astronomy, Department of at DigitalCommons@University of Nebraska - Lincoln. It has been accepted for inclusion in Theses, Dissertations, and Student Research: Department of Physics and Astronomy by an authorized administrator of DigitalCommons@University of Nebraska - Lincoln.

CHARACTERIZATION OF METAL-  
FERROELECTRIC-INSULATOR-SEMICONDUCTOR  
STRUCTURES BASED ON FERROELECTRIC  
LANGMUIR-BLODGETT POLYVINYLIDENE  
FLUORIDE COPOLYMER FILMS FOR  
NONDESTRUCTIVE RANDOM ACCESS MEMORY  
APPLICATIONS

by

Timothy James Reece

A DISSERTATION

Presented to the Faculty of The Graduate  
College at the University of Nebraska In  
Partial Fulfillment of Requirements For  
the Degree of Doctor of Philosophy

Major: Physics and Astronomy

Under the Supervision of Stephen Ducharme

Lincoln, Nebraska

December, 2007

CHARACTERIZATION OF METAL-  
FERROELECTRIC-INSULATOR-SEMICONDUCTOR  
STRUCTURES BASED ON FERROELECTRIC  
LANGMUIR-BLODGETT POLYVINYLIDENE  
FLUORIDE COPOLYMER FILMS FOR  
NONDESTRUCTIVE RANDOM ACCESS MEMORY  
APPLICATIONS

Timothy James Reece, Ph.D.

University of Nebraska, 2007

Advisor: Stephen Ducharme

Ferroelectric field effect transistors (FeFETs) have attracted much attention recently because of their ability to combine high speed, low power consumption, and fast nondestructive readout with the potential for high density nonvolatile memory. The polarization of the ferroelectric is used to switch the channel at the silicon surface between states of high and low conductance.

Among the ferroelectric thin films used in FET devices; the ferroelectric copolymer of Polyvinylidene fluoride, PVDF ( $C_2H_2F_2$ ), with trifluoroethylene, TrFE ( $C_2HF_3$ ), has distinct advantages, including low dielectric constant, low processing temperature, low cost and compatibility with organic semiconductors. By employing the Langmuir-Blodgett technique, films as thin as 1.8 nm can be deposited, reducing the operating voltage. An MFIS structure consisting of aluminum, 170 nm P(VDF-TrFE), 100 nm silicon oxide and n-type silicon exhibited low leakage current ( $\sim 1 \times 10^{-8}$  A/cm<sup>2</sup>), a large memory window (4.2 V) and operated at 35 Volts. The operating voltage was lowered through use of high k insulators like cerium oxide. A sample consisting of 25 nm P(VDF-TrFE), 30 nm cerium oxide and p-type silicon exhibited a 1.9 V window with 7 Volt gate amplitude. The leakage current in this case was considerably higher ( $1 \times 10^{-6}$

A/cm<sup>2</sup>). The characterization, modeling, and fabrication of metal-ferroelectric-insulator semiconductor (MFIS) structures based on these films are discussed.

## TABLE OF CONTENTS

I.	Basic Device Properties of Ferroelectric Langmuir-Blodgett Copolymer Films
1.1.	Ferroelectric Hysteresis
1.2.	Ferroelectric Polymers
1.3.	Langmuir Blodgett Technique
II.	Sample Preparation and Diagnostics of Langmuir-Blodgett Metal-Ferroelectric-Metal (MFM) Thin Film Capacitors
2.1.	Sample Preparation
2.2.	Experimental Techniques
2.3.	Dielectric Measurements
2.4.	The Sawyer Tower Method
2.5.	Pyroelectric Measurements
2.6.	Piezoelectric Measurements
III.	Introduction to the Metal-Ferroelectric-Insulator-Semiconductor (MFIS) Field Effect Transistor
3.1	Operating Modes of the MFIS Capacitor
3.2	Small Signal Capacitance Voltage Characteristics of the MOS Capacitor
3.3	Modeling the MFIS Capacitor
3.4	Non-Ideal Effects
IV.	Current Status of Metal-Ferroelectric-Insulator-Semiconductor (MFIS) Structures
4.1	The Floating Gate Transistor
4.2	MFIS State Retention
4.3	Perovskite Ferroelectrics in MFIS Structures
4.4	PVDF Copolymers in MFIS Structures
V.	Fabrication and Analysis of MFIS Structures Based on Langmuir-Blodgett Copolymer Films
5.1	Sample Preparation
5.2	Effective Trapped Charge
5.3	Capacitance-Voltage Characteristics
5.4	State Retention
5.5	Pyroelectric Measurements
5.6	Sawyer-Tower Measurements
5.7	Copolymer MFIS Structures with High Dielectric Constant Insulators

## ACKNOWLEDGMENTS

I would like to express my special gratitude to my advisor Professor Stephen Ducharme for granting me the opportunity to pursue a Ph. D. degree at UNL. His advice, insight and experience was invaluable and vital to the completion of this work.

I am grateful to my mother, sister, friends and family for their love and support.

A special thanks is given to Prof. Hermann Kohlstedt and Dr. Andreas Gerber. I benefited greatly from our occasional discussions pertaining to ferroelectric field effect transistors.

I am deeply indebted to Dr. Matthew Poulsen for our many discussions pertaining to ferroelectric Langmuir Blodgett films, his troubleshooting skills, and his assistance with many tasks.

A special thanks is given to Dr. Alexander Sorokin for his expert recommendations in regards to Langmuir Blodgett deposition techniques. His willingness to aid me with general deposition protocols made possible the fabrication of films of excellent quality.

I would like to thank Professor Ned Ianno for his expert advice in regards to semiconductor device physics and device processing in general.

I would also like to thank Dr. Mengjun Bai, Dr. Christina Othon, Mr. Brad Petersen, Mrs. Kristin Kraemer, Miss Jihee Kim, Mr. Ben Plowman, Dr. Rafal Korlacki, and Mr. Travis Johnson for being good friends and colleagues and for generously sharing laboratory equipment.

This work was made possible by support from the Nebraska Research Initiative, the Office of Naval Research, and the National Science Foundation.

## *Chapter 1*

### BASIC DEVICE PROPERTIES OF FERROELECTRIC LANGMUIR-BLODGETT POLYMER FILMS

#### 1.1 FERROELECTRIC HYSTERESIS

A material is said to be ferroelectric when it has a spontaneous polarization and at least two stable polarization states in the absence of an external electric field and can be shifted from one to another by a sufficiently large field known as the coercive field.<sup>1</sup> The polarization states form a basis for Boolean code and the stability of these states make ferroelectric materials attractive for use in nonvolatile memories. This chapter is meant to describe the characteristics of Langmuir-Blodgett ferroelectric polymer thin films, with emphasis on those properties that are particularly meaningful for device applications.

From an applications standpoint, the major properties of a ferroelectric are determined by the polarization-electric field (P-E) hysteresis loop (fig. 1). When a relatively large positive electric field ( $E_{sat}$ ) is applied to a new sample, all the dipoles align to form the saturated net polarization,  $P_s$  (point A in the figure). Since this polarization state is thermodynamically stable, a remanent polarization state,  $P_r$ , is evident even when the positive field is removed (point B). When a sufficient negative field is applied, the polarization state can be switched from positive to negative. The field at which the polarization crosses zero on the hysteresis loop is the coercive field,  $E_c$  (see point C on the figure). At point D on the figure, the dipoles are aligned again and saturated in the negative direction.

The four parameters of the hysteresis loop ( $E_c$ ,  $E_s$ ,  $P_r$ ,  $P_s$ ) determine many of the operating limits for a ferroelectric material. It should be noted that these are dependent on the frequency



of the loop as well as temperature. When the maximum applied field is less than the saturation value,  $E_s$ , the ferroelectric is said to be on a minor hysteresis loop, and its polarization states can be less stable than a saturated material.

From a device perspective, it is important to mention two important failure mechanisms of a ferroelectric film, fatigue and imprint. Fatigue is caused after switching the polarization of the ferroelectric a large number of cycles. This results in a drop in the remanent polarization due to degradation of the film. The damage is permanent in this case. In the case of imprint, the ferroelectric, after being polarized in one state, tends to prefer this over the other state and shows a hysteresis loop that is shifted to the left (right) when polarized in the positive (negative) state. In this case, a refresh can restore the initial hysteresis. In both cases, improvement in the interfaces with electrodes reduces the problems to a certain degree.

The essential bistability in the permanent electric polarization of a ferroelectric thin film can be exploited to make a nonvolatile memory device described as ferroelectric random access memory (FRAM). Available devices (smart cards and cache chips)<sup>2</sup> are based on perovskite ferroelectrics such as lead zirconate-titanate (PZT) or strontium barium titanate (SBT).<sup>3</sup> Ferroelectric memories in current use employ a destructive readout scheme, memory function is performed by electrically switching between two states in a ferroelectric capacitor structure. Loss of written data at one polarization state in a readout operation requires restoration by a rewrite cycle. This increases access time, limits operational lifetime, and affects memory cell area in order to accommodate the additional circuitry.<sup>4-6</sup> Current read and write operations in perovskite FRAMs take approximately 1 microsecond, use approximately 1 nJ per bit, and can last  $\sim 10^{10}$  cycles. In contrast, current technologies are much slower and require much more energy-electrically erasable programmable read-only memory (EEPROM) requires 10

microseconds and 1 microJ and Flash requires  $\sim 500$  microsecond and 2 microJ for a lifetime of  $\sim 10^6$  cycles. In developing commercially viable devices, researchers overcame many difficult hurdles, most notably film degradation ('fatigue') after repeated switching due to chemical instabilities in the films and at the interfaces.<sup>7-9</sup> Another drawback is that perovskites generally require annealing at temperatures that are too high for the advanced logic large-scale integrated circuits (LSIs) fabricated with a design rule finer than 45 nm.<sup>10</sup> However, new formulations should reduce the annealing temperature significantly to improve compatibility.

## 1.2 FERROELECTRIC POLYMERS

Another promising material class for use in nonvolatile memories is ferroelectric polymers, such as polyvinylidene fluoride (PVDF, consisting of  $C_2H_2F_2$  monomers) and its copolymers with trifluoroethylene (TrFE,  $C_2HF_3$ ). The VDF copolymers have a large spontaneous polarization, approximately  $0.1 \text{ C/m}^2$ , excellent polarization stability, and switching times as short as 0.1 microsecond. Their high resistivity of up to 1000 ohm-cm means low leakage, suitable for non-destructive readout applications. Further, they do not require high-temperature processing ( $T_c < 200^\circ\text{C}$ ), have outstanding chemical stability, low fabrication costs, and are non-toxic.

In the case of PVDF, the manner in which the molecular constituents are linked greatly affects the macroscopic properties of the polymer. Torsional rotations about single bonds determine the specific chain conformation of the polymer. The most favorable torsional bond arrangements have substituents at  $180^\circ$  to each other (called trans or t) or at  $\pm 60^\circ$  (called gauche<sup>±</sup> or g<sup>±</sup>).<sup>11</sup> The two most common conformations for PVDF are all-trans (tttt) and alternating trans-gauche (tg<sup>+</sup>tg<sup>-</sup>). The all-trans conformation places the hydrogen and fluorine

atoms on opposite sides of the carbon chain, resulting in a large dipole moment nearly perpendicular to the chain axis. The ordered trans-gauche conformation is less polar, having significant dipole components both perpendicular and parallel to the axis of the chain.

The net polarization of the crystal is also dependent on chain packing. The trans-gauche molecules can be packed in such a way that the dipole moments are cancelled out. This is the paraelectric ( $\alpha$ ) phase of PVDF. On the other hand, the unit cell of the ferroelectric ( $\beta$ ) phase, shown in fig. 2, consists of two all-trans chains packed with dipole moments pointing in the same direction.<sup>11</sup>

Both piezoelectricity and pyroelectricity were observed over thirty years ago in poly-(vinylidene fluoride) (PVDF). Although PVDF shows clear, repeatable, polarization hysteresis, there was doubt initially that this was of ferroelectric origin because many polymers exhibit long-lived but transient hysteresis due to either charge injection or induced polarization. The unambiguous evidence that hysteresis was due to ferroelectric switching came from the synthesis and systematic study of the copolymers with trifluoroethylene (TrFE) and tetrafluoroethylene (TeFE).<sup>14</sup> The substitution of either TrFE or TeFE suppresses the ferroelectric-paraelectric phase transition temperature below the melting point, thus providing a direct connection between switching charge and the appearance of a spontaneous polarization.

### Temperature Considerations

The thermal properties of the ferroelectric copolymer LB films present unique challenges and opportunities. The key temperatures for the VDF copolymers are the phase transition temperature  $T_C$  and the melting point  $T_M$ . Fig. 3 shows the phase diagram of the VDF-TrFE

copolymer system. The melting point  $T_M$  varies from a high of 179 °C for PVDF through a low of 148 °C for the 80:20 copolymer to 166 °C for PTrFE, while the phase transition temperature  $T_C$  decreases steadily from over 200 °C (extrapolated) for PVDF. So far, the highest molar content of TrFE with observed ferroelectricity is 63 mol. %.<sup>13</sup>

The films must be annealed, once, at above the transition temperature  $T_C$ , but below  $T_M$  to improve crystallinity. The films must not be heated above the melting point  $T_M$  or much or all crystallinity will be permanently lost. The film polarization decreases sharply as the temperature nears  $T_C$ , but data is not necessarily lost unless the film temperature exceeds the transition temperature  $T_C$ . A composition of 80% VDF would seem a good choice for manufacturing as the transition temperature  $T_M \approx 145$  °C should be high enough for storage and operating conditions and enough below the melting point  $T_M \approx 148$  °C to allow for proper annealing in the paraelectric phase. The relatively low melting point, and the fact that melting may destroy the device, places the tightest constraints on chip packaging, post-processing, and assembly conditions. Table I lists properties of PVDF and the 70:30, 80:20 polymers.

### Sample Preparation

Traditionally, ferroelectric polymer samples are prepared as follows. The polymer is synthesized and dispersed in solution, usually in a polar solvent. The solution is then formed by casting or spinning and the solvent evaporated, leaving a pliable solid sample that is typically polymorphous- an inhomogeneous mixture of amorphous and crystalline material. The crystallites can have multiple structures and usually have lamellar morphology with dimensions of order 50 nm by 500 nm by 5 nm. The lamellae are microscopically ferroelectric, with in-plane polarization. To improve crystallinity and produce macroscopic polarization, the

polymorphous samples are heated and drawn to ratios of 3:1 or more and poled by applying a large voltage across two faces. By these means it is generally possible to obtain ~50% crystallinity and ~25% polarization with PVDF and over 90% crystallinity and 80% polarization with copolymers near containing approximately 20-40% TrFE.<sup>14</sup> Just over 10 years ago, the group at Yamagata University led by Ohigashi developed techniques for producing essentially 100% crystallinity and highly twinned, but optically clear, crystals several hundred microns thick, an impressive achievement.<sup>21,22</sup> Another notable innovation is the growth by vapor deposition of epitaxial crystalline films of VDF oligomers by a group at Kyoto University.<sup>23</sup> The oligomer films are likely ferroelectric as they exhibit reversible switching with bits sizes as small as 30 nm written by Atomic Force Microscopy (AFM).<sup>24</sup>

### 1.3 LANGMUIR-BLODGETT TECHNIQUE

The Langmuir-Blodgett technique is a means of depositing uniform molecular molecules on solid substrates. Typically, monolayer forming molecules consist of two regions within the molecule: a hydrophilic polar 'head', which is soluble in water, and a hydrophobic alkyl 'tail', which is not soluble. This material is dissolved in a highly volatile, subphase-immiscible solvent and dispersed dropwise onto a trough filled with the subphase liquid, forming a monomolecular layer on the surface. This Langmuir layer may be transferred onto a substrate, which passes through the layer or contacts it horizontally. The repeated transfer of the monolayer film from the subphase surface to a suitable solid substrate produces a multilayer thin film called a Langmuir-Blodgett (LB) film. The ability to control the thickness on a molecular level is the most prominent feature of this technique. LB film thickness is precisely determined by the thickness of a single layer and the number of transfers (vertical dipping results in two transfers, one for each horizontal dip).

Although PVDF and its copolymers are not good amphiphiles and require solvents that are miscible in water, it turns out that due to the large molecular weight of polymers, these can be dispersed to form a sufficiently stable Langmuir layer on water with a repeatable pressure area isotherm as shown in Fig. 4. PVDF and related polymers are not very soluble in volatile and water-immiscible solvents that are frequently used in LB deposition. These polymers are more soluble in polar solvents, such as acetone and dimethyl sulfoxide (DMSO), which are miscible with water, reducing the efficiency of film dispersal. The polar solvents carry much of the polymer into the water solution; only about 10% of the polymer remains on the surface. The effects of a water-miscible solvent may be minimized by reducing the size and speed of solution droplets as they are introduced onto the subphase surface. Because the polymer is not a good amphiphile, the film on the trough may not be a true monolayer, and tends to produce somewhat thicker films per nominal monolayer (ML) ( $1.78 \pm 0.07$  nm for 70:30 PVDF-TrFE), about 2-3 times the molecular diameter.<sup>25</sup>

This method produces highly ordered LB multilayer films with the chains laying parallel to the surface, as verified by theta-2-theta X-ray diffraction, which measures the (110) close-packing peak perpendicular to the layers.<sup>26</sup> This means that the polarization, which is along the (010) direction,<sup>27</sup> is tilted about the chain axis  $30^\circ$  away from the film normal. The films then are crystalline mosaics, with uniform orientation normal to the substrate but disordered in-plane orientation.<sup>28</sup> The films often require thermal annealing in the paraelectric phase (100-150 °C for 70:30 copolymer), with best results from annealing close to but below the melting point.<sup>29</sup>

Film Morphology is readily probed by Scanning Electron Microscopy (SEM), Atomic Force Microscopy (AFM), STM, and Optical Interference Profilometry (OIP).<sup>26</sup> The SEM studies of copolymer LB films deposited on electronic-grade silicon are predominately planar with about

~5% of the surface consist of ‘tectonic’ features as seen in Fig. 5.<sup>30</sup> The mountain ridges appear to be a result of compression stresses that cause local collapse, even at low (~5 mN/m) Langmuir layer surface pressures. Since electrodes with  $\geq 1 \text{ mm}^2$  area are routinely used, these ridges have minimal effect on measurements. The ridges are a concern for integrated device applications, as they will result in a significant number of failed devices. The STM images routinely reveal highly planar and ordered arrays of straight polymer chains, but these images are not necessarily representative.<sup>31</sup> The AFM and OIP images generally confirm the planar nature on a length scale of microns.<sup>26</sup>

### Cell Size

The minimum cell area is fundamentally limited by the minimum stable size domain and possibly by cross-talk interactions. The absolute minimum domain size for continuous ferroelectric LB copolymer films has not been established, but preliminary AFM studies showed that stable and reversible polarization features 200 nm across and 20 nm thick could be written and measured.<sup>32</sup> A group at Kyoto University has demonstrated 30 nm bits and 100 nm bit spacing in copolymer films deposited on Pt by spin coating, using AFM and electric force microscopy.<sup>33</sup> An encouraging result is the reported polarization manipulation on the nanometer scale in LB copolymer films (Fig. 6), caused by switching the polarity of a scanning tunneling microscope (STM) tip.<sup>34</sup> Other evidence comes from the discovery that the copolymer films spontaneously form isolated nanomesas about 120 nm in diameter and 7 nm thick.<sup>35</sup> These are disk-shaped, fairly uniform in size, and highly crystalline, with (110) orientation of the all-trans  $\beta$  phase just like in continuous films.

### Switching Speed

The kinetics of polarization switching in the ferroelectric polymer LB films exhibit critical behavior; there is a pronounced slowing just above the coercive field and just below the critical temperature. The critical slowing is observed in the switching kinetics of ferroelectric Langmuir-Blodgett films of 70% vinylidene-fluoride and 30% trifluoroethylene copolymer with thickness up to 15 nm. This very slow switching (on the order of seconds) of the thinnest LB films presents a major impediment to nonvolatile random-access memory applications. For this reason, samples in this study will be limited to thicker films (on the order of 20 LB deposition steps) where the dominant switching mechanism is extrinsic switching.

Extrinsic switching, which has been identified as the dominant mechanism from the earliest studies, is an activated process characterized by an exponential increase in switching rate (reciprocal switching time  $\frac{1}{\tau}$ ) with increased temperature  $T$  and electric field  $E$  of the empirically-determined form (in the nucleation-limited case)<sup>36-38</sup>

$$\frac{1}{\tau} \propto \exp \left[ \frac{-\left(\frac{c}{T} + b\right)}{E} \right] \quad (1.1)$$

where  $\tau$ ,  $b$  and  $c$  are constants. Extrinsic switching is usually achieved with external fields in the range 0.1 to 50 MV/m.<sup>39</sup> Strictly speaking, extrinsic switching does not have a true threshold coercive field because the activation of nucleation permits switching at arbitrarily small fields, given enough time, but switching experiments are typically carried out with an ac field and so the apparent coercive field is actually a function of frequency.<sup>40</sup> Further, intrinsic switching rates in thin films generally follow an approximately  $-0.7$  power law dependence on thickness, which is variously attributed to scaling of nucleation rates or to domain wall velocities.<sup>41</sup> Thin films of PVDF and its copolymers made by solvent methods have low



coercive fields  $< 50$  MV/m. Switching times, as small as 100 ns, closely follow the exponential dependence of switching rate on field and temperature given in Eq. 1.1 over many decades.<sup>18</sup>

## References

1. M. E. Lines and A. M. Glass, *Principles and Applications of Ferroelectrics and Related Materials* (Clarendon, Oxford, 1977), 680 Pages.
2. J. F. Scott, *Ferroelectric Memories* (Springer-Verlag, Berlin, 2000), 190 Pages.
3. O. Auciello, J. F. Scott, and R. Ramesh, *Phys. Today* **51**, 22-7 (1998).
4. A. Shiekholeslami and P. G. Gilak, *Proc. IEEE* **88**, 667 (2000).
5. K. Sugibushi, Y. Kurogi, and N. Endo, *J. Appl. Phys.* **46** (7), 2877 (1975).
6. K. Asari et al., *IEICE Trans. Electron.* E81-c, 488 (1998).
7. S. Thakoor and A. P. Thakoor, *Appl. Opt.* **34**, 3136 (1995).
8. R. Moazzami, *Semicond. Sci. Tech.* **10**, 375 (1995).
9. C. A. Paz de Araujo, J. D. Cuchiaro, L. D. McMillan, M. C. Scott, and J. F. Scott, *Nature* **374**, 627-9 (1995).
10. S. Fujisaki, H. Ishiwara, Y. Fujisaki, *Appl. Phys. Lett.* **90**, 162902 (2007).
11. A. J. Lovinger, *Science* **220**, 1115 (1983).
12. K. Koga and H. Ohigashi, *J. Appl. Phys.* **59**, 2142-50 (1986).
13. H. Kodama, Y. Takahashi, and T. Furukawa, *Japanese Journal of Applied Physics, Part I (Regular Papers, Short Notes & Review Papers)* **38**, 3589-95 (1999).
14. T. Furukawa, *Phase Transitions* **18**, 143-211 (1989).
15. S. Ducharme, S. P. Palto, and V. M. Fridkin, "Ferroelectric Polymer Langmuir-Blodgett Films," in *Ferroelectric and Dielectric Thin Films*, H. S. Nalwa, ed. (Academic Press, San Diego, 2002).
16. K. Koga, N. Nakano, T. Hattori, and H. Ohigashi, *J. Appl. Phys.* **67**, 965-74 (1990).
17. K. Kimura and H. Ohigashi, *Jpn. J. Appl. Phys.* **25**, 383-7 (1986).
18. T. Furukawa, H. Matsuzaki, M. Shiina, and Y. Tajitsu, *Jpn. J. Appl. Phys.* **24**, L661-L2 (1985).
19. S. Ducharme, S. P. Palto, L. M. Blinov, and V. M. Fridkin, "Physics of Two-Dimensional Ferroelectric Polymers," in *Proceedings of the Fundamental Physics of Ferroelectrics*, R. E. Cohen, ed. Vol. **535** (American Institute of Physics, Aspen, CO, 2000), pp. 354-63.
20. G. Vizdrik, S. Ducharme, V. a. M. Fridkin, and S. G. Yudin, *Phys. Rev. B* **68**, 94113 (2003).
21. M. Hikosaka, K. Sakurai, H. Ohigashi, and T. Koizumi, *Jpn. J. Appl. Phys.* **32**, 2029-36 (1993).
22. H. Ohigashi, K. Omote, and T. Gomyo, *Appl. Phys. Lett.* **66**, 3281-3 (1995).
23. K. Noda, K. Ishida, T. Horiuchi, K. Matsushige, and A. Kubono, *J. Appl. Phys.* **86**, (1999).
24. K. Noda, K. Ishida, A. Kubono, T. Horiuchi, H. Yamada, and K. Matsushige, *Japanese Journal of Applied Physics, Part I (Regular Papers, Short Notes & Review Papers)* **40**, (2001).
25. M. Bai, A. V. Sorokin, D. W. Thompson, M. Poulsen, S. Ducharme, *J. Appl. Phys.* **95**, 3372 (2004).
26. M. Bai, M. Poulsen, A. V. Sorokin, S. Ducharme, and V. M. Fridkin, in *Proceedings of the Electroactive Polymers and Their Applications as Actuators, Sensors, and Artificial Muscles*, Nov. 26-30, 2001, Q. Zhang, E. Fukada, Y. Bar-Cohen, and S. Bauer, eds., Vol. **698** (Materials Research Society, Boston, 2002), pp. CC10.4.1-6.
27. J. Choi, C. N. Borca, P. A. Dowben, A. Bune, M. Poulsen, S. Pebley, S. Adenwalla, S. Ducharme, L. Robertson, V. M. Fridkin, S. P. Palto, N. N. Petukhova, and S. G. Yudin, *Phys. Rev. B* **61**, 5760-70 (2000).
28. M. Bai, "The Structure of Ferroelectric PVDF/TrFE Copolymer Langmuir-Blodgett Films," PhD, (University of Nebraska, 2002).

29. M. Poulsen, S. Adenwalla, S. Ducharme, V. M. Fridkin, S. P. Palto, N. N. Petukhova, and S. G. Yudin, in *Proceedings of the Ferroelectric Thin Films IX*, Nov. 27-Dec. 1, S. R. G. P.C. McIntyre, Y. Miyasaka, R.W. Schwartz, D. Wouters, ed. Vol. **655** (Materials Research Society, Boston, 2000), pp. CC10.4.1-6.
30. S. Ducharme, M. Bai, M. Poulsen, S. Adenwalla, S. P. Palto, L. M. Blinov, and V. M. Fridkin, *Ferro.* **252**, 191-9 (2001)
31. A. V. Bune, V. M. Fridkin, S. Ducharme, L. M. Blinov, S. P. Palto, A. V. Sorokin, S. G. Yudin, and A. Zlatkin, *Nature* **391**, 874-7 (1998).
32. L. M. Blinov, R. Barberi, S. P. Palto, M. P. De Santo, and S. G. Yudin, *J. Appl. Phys.* **89**, 3960-6 (2001).
33. K. Matsushige, H. Yamada, H. Tanaka, T. Horiuchi, and X. Q. Chen, *Nanotechnology* **9**, 208-11 (1998).
34. H. Qu, W. Yao, T. Garcia, J. Zhang, A. V. Sorokin, S. Ducharme, P. A. Dowben, V. M. Fridkin, *Appl. Phys. Lett.* **82**, 4322 (2003).
35. J. Li, Y. Luo, M. Bai, S. Ducharme, *Appl. Phys. Lett.* **87**, 213116 (2005).
36. W. J. Merz, *Phys. Rev.* **95**, 690 (1954).
37. E. Fatuzzo and W. J. Merz, *Phys. Rev.* **116**, 61 (1959).
38. E. Fatuzzo, *Phys. Rev.* **127**, 1999-2005 (1962).
39. V. M. Fridkin and S. Ducharme, *Phys. Solid State* **43**, 1320-24 (2001).
40. W. J. Merz, *J. Appl. Phys.* **27**, 938-43 (1956).
41. H. L. Stadler and P. J. Zachmanidis, *J. Appl. Phys.* **34**, 3255-60 (1963).

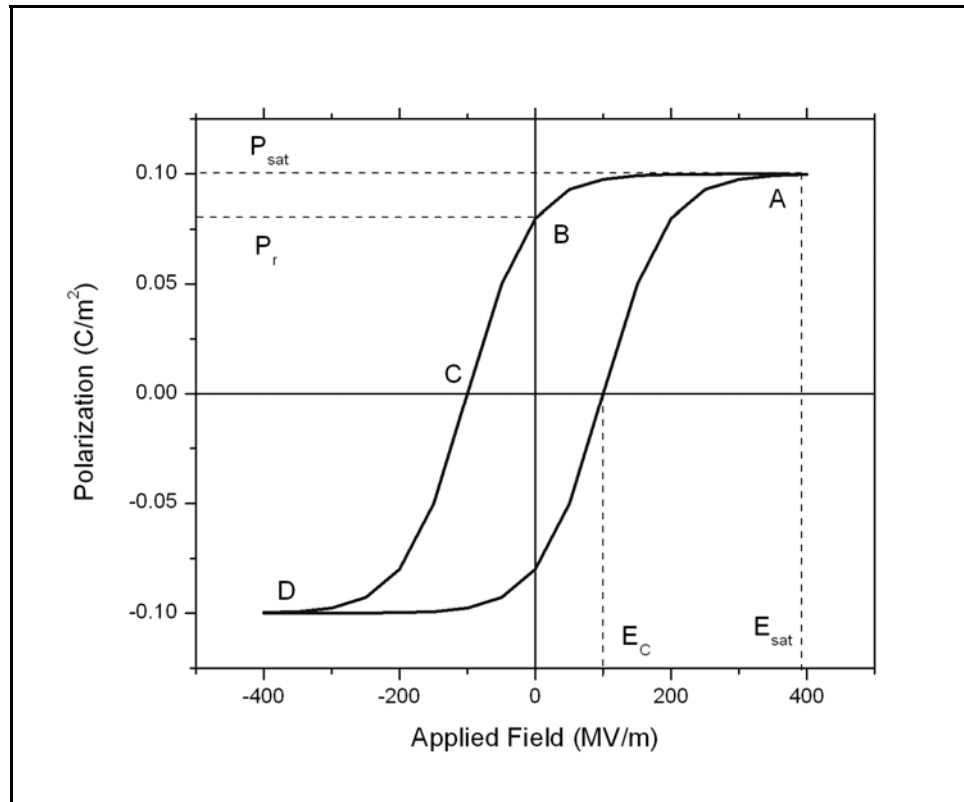


Fig. 1.1 Sketch of a polarization versus applied field (P-E) hysteresis loop of a ferroelectric material.

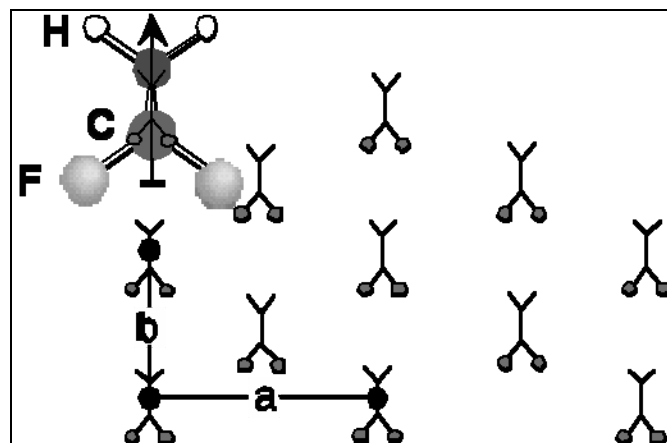


Fig. 1.2 Crystal structure of the ferroelectric phase for PVDF, chains viewed end-on.

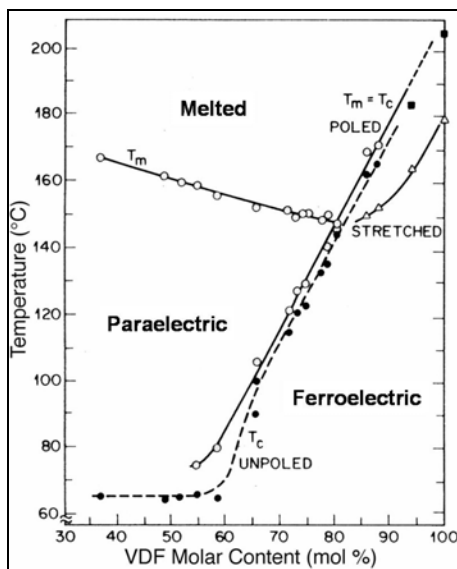


Fig. 1.3 Phase diagram of the PVDF-TrFE copolymer system. Reprinted with permission from [16]. Copyright [1990], American Institute of Physics.

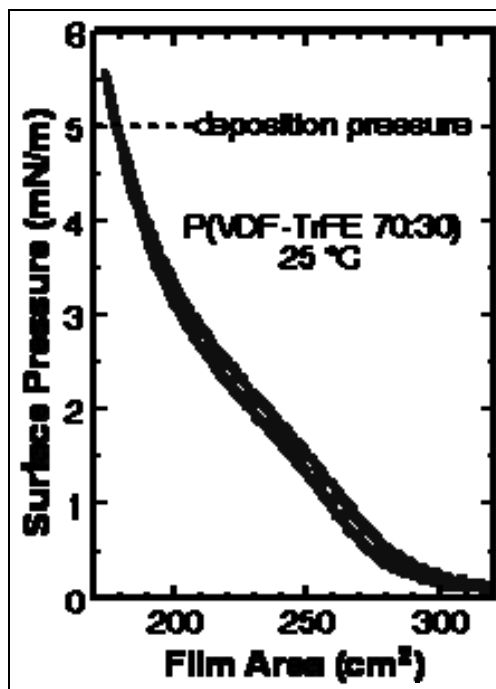


Fig. 1.4 Pressure-Area isotherm formed from a 0.01% solution of the 70:30 copolymer in Dimethyl Sulfoxide (DMSO).

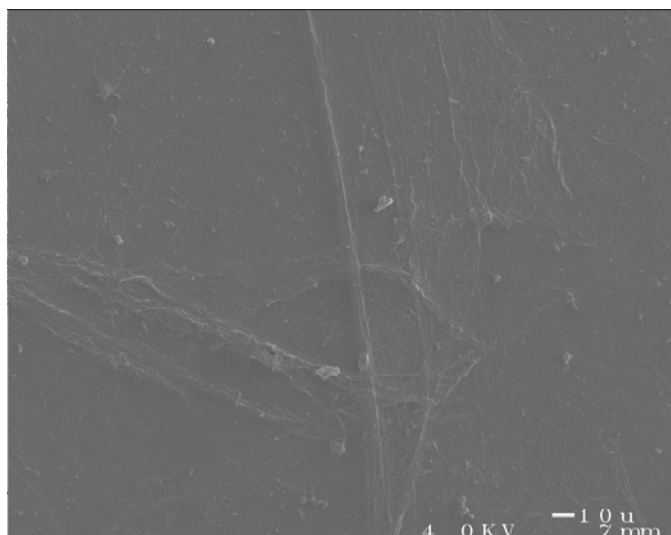


Fig. 1.5 Scanning Electron Microscope (SEM) image of a 50 ML LB film on silicon.<sup>30</sup>

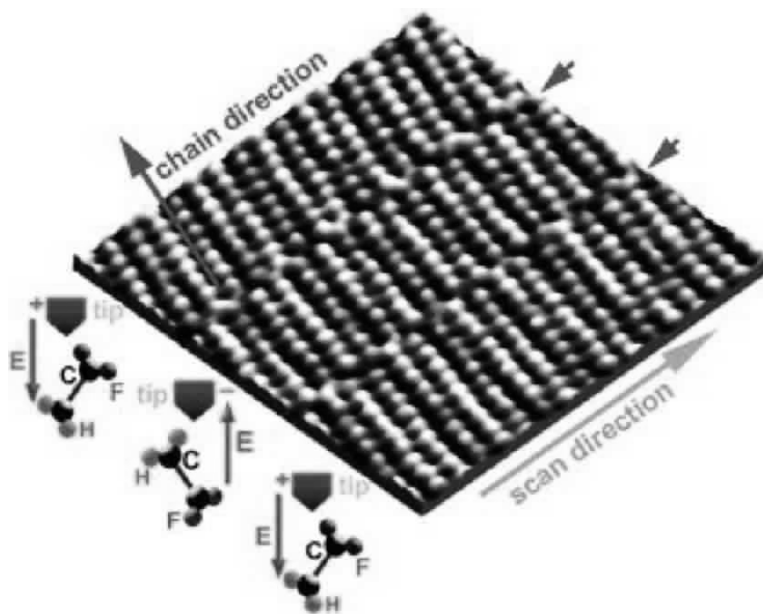


Fig. 1.6 Scanning Electron Microscope (SEM) image of a 2 ML film showing regions manipulated the polarity of the tip. Dimensions are 4.4 nm by 4.4 nm. Reprinted with permission from [34]. Copyright [2003], American Institute of Physics.

Table I: Properties of PVDF and some of its copolymers.<sup>14</sup>

Property	PVDF	80:20 Copolymer	70:30 Copolymer	<b>70:30 Copolymer LB Films<sup>15</sup></b>
Melting Temperature <sup>12</sup>	180 °C	148 °C	152 °C	>150 °C
Transition Temperature <sup>12</sup>	N.A.	145 °C	116 °C	80 °C (cooling) 110 °C (heating)
Dielectric Constant	16	12	10	>8
Remanent Polarization	12 $\mu\text{C}/\text{cm}^2$	10 $\mu\text{C}/\text{cm}^2$	8 $\mu\text{C}/\text{cm}^2$	$\sim 8 \mu\text{C}/\text{cm}^2$
Coercive Field	75 (MV/m) <sup>16</sup>	38 (MV/m) <sup>16</sup>	5-60 (MV/m) <sup>17</sup>	50-500 MV/m
Switching Speed at Field			0.1 $\mu\text{s}$ at 300 MV/m to 15 ms at 6 MV/m <sup>18</sup>	2 $\mu\text{s}$ <sup>19</sup> to >1200 s <sup>20</sup>

## *Chapter 2*

### SAMPLE PREPARATION AND DIAGNOSTICS OF LANGMUIR-BLODGETT METAL-FERROELECTRIC-METAL THIN FILM CAPACITORS

#### 2.1 SAMPLE PREPARATION

Metal-ferroelectric-metal capacitor samples that were used to probe the ferroelectric properties of the polymer films were made on 1 in.<sup>2</sup> glass slides. Two to three bottom electrodes consisting of aluminum stripes with 1 mm width and 100 nm thickness were deposited by vacuum thermal evaporation at a chamber pressure of  $5 \times 10^{-5}$  mbar using a Bal-tec MED 020 coating system. Aluminum was chosen because it is cheaper than most metals and easy to evaporate. Additionally, PVDF-TrFE LB copolymer films seem to adhere better to metals with an oxide layer. The thickness of the electrodes was determined using a Sycon STM/MF thickness/rate monitor. The deposition rate of the electrodes ranged from 1 to 2 Å/sec.

Subsequently, the Langmuir layer is dispersed dropwise on an ultrapure (18 MΩ-cm) water subphase from a 0.01%-0.05% solution of the 70:30 PVDF:TrFE copolymer in DMSO (unless otherwise noted). The approximately 50 µL drops were dispersed at a rate of 2-4 per minute until approximately 1 mL of solution is applied to the 1200 cm<sup>2</sup> area of the NIMA Technologies Teflon<sup>TM</sup> LB trough. Rather than dripping the droplets directly from a syringe, these were allowed to drain slowly over a slightly inclined glass slide. The layer was allowed to sit for a half hour to provide sufficient time for the solvent to evaporate. The surface layer is then compressed by closing the trough perimeter barriers slowly until the solid phase surface pressure of 5 mN/m is achieved and this pressure is maintained throughout the deposition process. The Langmuir-Blodgett film is deposited at a constant subphase temperature of 25°C



controlled by the flow of water beneath the surface of the trough using an Isotemp refrigerated circulator. Deposition is made through the Schaefer variation on the Langmuir-Blodgett technique. This is achieved by lowering the substrate nearly horizontal to the surface layer using a tilt angle of 5-7 degrees to avoid the formation and trapping of air bubbles and to ensure smooth film adhesion. After the substrate touches water, the tilt angle is slowly reduced to zero and then tilted back at about  $\frac{1}{2}$  degree per second and withdrawn slowly so that the meniscus line withdraws across the substrate slowly enough to prevent significant strain or damage to the film. The substrate is then allowed to dry between layers for an amount of 5 minutes for the first 5 layers and less than a minute thereafter.

Aluminum top electrode stripes were then deposited in the same fashion as (but perpendicular to) the bottom electrodes. Each capacitor in the cross point array is electrically isolated from the others by scratching the electrodes.

#### Thermal treatment

Thermal annealing is often used to improve the crystallinity of polymeric materials. For LB film formation, most films benefit from thermal annealing. Samples are annealed in the paraelectric phase, where the crystalline axes are expanded, increasing the mobility. It is believed that the molecular chains undergo local reorganization due to thermal fluctuations in the paraelectric phase.<sup>1</sup> Below the ferroelectric-paraelectric phase transition, the process may be very slow due to low chain mobility. This may explain why better crystallinity is achieved in copolymer films,<sup>2</sup> compared to pure PVDF, which melts before the phase transition temperature can be reached.

All P(VDF-TrFE) films used in this study were annealed to improve crystallinity prior to measurements. Samples were heated at a rate of 1 °C/min. in an isolated copper chamber up to a temperature of 120 °C. The temperature was kept at this value for at least an hour and then cooled at a rate of 1 °C/min. back down to room temperature.

## 2.2 EXPERIMENTAL TECHNIQUES

### Dielectric Measurements

A number of different techniques were employed to probe the switching characteristics of the ferroelectric copolymer films. Dielectric measurements,  $C(E) \propto \frac{dD}{dE}$ , were particularly convenient because they yield an estimate for the film thickness and provide an estimate for the saturation and coercive fields. Small signal capacitance-voltage sweeps show hysteresis and form so-called ‘butterfly’ curves (Fig. 2.1). Since film capacitance is at a maximum when the change in polarization is greatest, the voltage at which the capacitance peak occurs in the butterfly loop provides an approximation for the coercive voltage. Furthermore, when the applied voltage is high enough to saturate the film, the butterfly curves appear to “pinch” off at the peak voltages.

Measurements were made using an impedance analyzer (Hewlett-Packard 4192A) with a small test signal of 0.1 V at 1 kHz frequency. To measure the curves, the voltage was ramped at 0.05 V/sec with 0.1 V steps while simultaneously measuring the capacitance on the impedance analyzer. Typically, multiple cycles were measured in order to check repeatability of loops. Measurements were made while the samples were kept at room temperature, 30°C.

Fig. 2.2 shows the “butterfly” curve coercive and saturation voltages for 70:30 copolymer films of various thicknesses. Assuming a LB thickness deposition rate of 1.7 nm/layer, these values

correspond to  $E_c = 75 \frac{MV}{m}$  and  $E_{SAT} = 510 \frac{MV}{m}$  for the thinnest films in this study (20 nm).

While the thickest films (approximately 100 nm), have lower average values of

$$E_c = 63 \frac{MV}{m} \text{ and } E_{SAT} = 210 \frac{MV}{m}.$$

### The Sawyer Tower Technique

The standard circuit for measuring ferroelectric hysteresis is called the Sawyer Tower circuit.<sup>3</sup>

The specific circuit used in this study is shown in Fig. 2.3. By measuring the voltage,  $V_{Load}$ , across a standard capacitor ( $C_{Load}$ ) in series with the ferroelectric sample ( $C_{Ferro}$ ), the charge on the ferroelectric can be determined since  $Q_{Ferro} = C_{Load} V_{Load}$ . The sine wave or bipolar triangular signal applied to the circuit is sent to the X channel of an X-Y trace of an oscilloscope. Most of this voltage drops across the ferroelectric since generally the capacitance of the load is chosen to be much greater than that of the sample. The Y signal is the voltage across the load capacitor, which is readily converted into the ferroelectric polarization  $P_{Ferro}$ :

$$C_{Load} V_{Load} = (\epsilon_0 \epsilon_{Ferro} E_{Ferro} + P_{Ferro}) A_{Ferro} \quad (2.1)$$

where  $\epsilon_{Ferro}$ ,  $E_{Ferro}$ ,  $P_{Ferro}$  and  $A_{Ferro}$  are the dielectric constant, electric field, polarization, and area of the ferroelectric capacitor respectively. Generally, the linear term on the right hand side is small in comparison to the second term and therefore it was ignored in this study.

Sawyer Tower polarization loops were measured by applying triangle and sine waveforms of various frequencies to the circuit using a Stanford Research Systems DS345 function generator. In cases where voltages above 10 V were needed, a voltage amplifier was added to the circuit. A 1  $\mu$ F capacitor was chosen for the load capacitor, since the capacitances of all of the ferroelectric capacitors in this study were at least 3 orders of magnitude less than this value, ensuring that only a small portion of the applied voltage was lost to the load. A Tektronix 2440 digital oscilloscope was used to record the applied voltage (x channel) and voltage drop across the load capacitor (y channel).

Polarization loops for a 30 ML film taken at various waveform frequencies are shown in Fig 2.4. The maximum polarization,  $P_{SAT} \approx 6 \frac{\mu C}{cm^2}$ , achieved for a 10 hz triangle waveform is slightly lower than normal values quoted for copolymer films,  $P_{SAT} \approx 10 \frac{\mu C}{cm^2}$ . The remanent polarization gradually decreases as the applied frequency increases, indicating that the film only partially switches at higher frequencies. This may be an indication that part of the film is amorphous.

Fig 2.5 and 2.6 show the average results of sawyer tower polarization data for samples of various thicknesses. For comparison, a 20 ML LB film that was formed using Acetone as the solvent is also included, since these films appeared to switch faster in previous studies. Films made using DMSO solvent seem to show the same frequency behavior in terms of the remanent polarization. The Acetone film is unique in that while the remanent polarization is lower than the other films at low frequency, the value does not drop off as much at higher frequencies. This trend is also true in the coercive voltage data. This seems to indicate that

films made using Acetone as the solvent are less crystalline, but a larger percentage of the film switches at high frequencies.

The Sawyer tower technique also provides a convenient method for measuring fatigue in ferroelectric films. Fig. 2.7 shows the effects of continual cycling on the hysteresis loop for a 20 ML LB film. The larger loop was measured with a 1 hz sine waveform while the sample was still rather fresh (only a few 100 cycles had been preformed on the film). The more closed loop was also taken at 1hz, but after 100 thousand cycles had been applied to the film at 100 hz. The plot shows a 34% reduction in the remanent polarization. These results seem consistent with recent fatigue studies involving  $\sim 1\text{ }\mu\text{m}$  thick spun films, which showed an approximately 50% drop off after 900 thousand cycles performed at 100 hz.<sup>4</sup> The measurements were also made at 1 hz test frequency, but a triangle waveform was used. This film fatigue may prove to be a stumbling block for memory applications using P(VDF-TrFE) copolymers.

### Pyroelectric Measurements

Pyroelectric measurements were conducted by using rapid laser modulation heating (the Chynowyth method).<sup>5,6</sup> In this method, the sample is heated by a Research Electro-Optics 5 mW (Helium-Neon) He-Ne laser chopped at a frequency of 2 khz (Fig. 2.8). The pyroelectric response of the sample was measured at zero bias after the application of a polarizing voltage using a Stanford Research Systems SR830 DSP lock-in amplifier referenced to the chopper frequency. The DC voltage was supplied by the Stanford Research Systems DS 345 function generator and a voltage amplifier was used when an offset bias larger than 5 V was needed. The film can expand or contract only perpendicular to the surface, because the thermal expansion coefficient of the substrate is at least one order of magnitude less than the thermal

expansion coefficient of the polymer,<sup>7</sup> so the measured pyroelectric coefficient consists of two contributions, the primary effect and the secondary effect:<sup>8</sup>

$$p_3(\text{eff}) = \left( \frac{\partial P_s}{\partial T} \right)_S + \frac{d_{33}^T \alpha_3^S}{s_{33}^S} = \left( \frac{I}{A} \right) \left( \frac{\partial T}{\partial t} \right)^{-1} \quad (2.2)$$

where  $P_s$  is the spontaneous polarization,  $T$  is the temperature,  $S$  is the strain,  $d_{33}^T$  is the stress free piezoelectric coefficient,  $s_{33}^S$  is the elastic compliance coefficient,  $\alpha_3^S$  is the thermal expansion coefficient,  $I$  is the pyroelectric current,  $A$  is the surface area, and  $\frac{\partial T}{\partial t}$  is the rate of temperature change. Since the pyroelectric response is directly proportional to the net sample polarization, this method can be used to measure remanent polarization hysteresis loops.

The pyroelectric current was measured by applying a long (1 min.) DC pulse to a sample, then removing the voltage and measuring the signal to the lock-in after about 30 seconds. Pyroelectric hysteresis loops like the one shown in Fig. 2.9 were achieved by repeating the process for many applied voltages. The solid curve in Fig. 2.9 indicates that the tanh function model (which will be described in detail in chapter 3 by Miller and McWhorter can be used to fit the pyroelectric data very well. Since the applied voltage is applied for a longer period of time and varied slowly in the pyroelectric set-up, the film saturates at a lower voltage and yields larger coercive fields than it does in the capacitance measurements.

The pyroelectric technique for probing the polarization state of the films provides a convenient and noninvasive method for determining retention properties. After a 40 ML film was saturated in the positive direction, it was placed in storage. After nearly 1.5 years, when the

signal was again measured under the same conditions, the signal was seen to drop only slightly, the new value was more than 75% of the previously recorded pyroelectric signal.

#### Piezoelectric measurements

All ferroelectrics exhibit the converse piezoelectric effect, the production of strain when an electric field is applied. A high resolution Mach-Zehnder interferometer was adopted to measure sample strain and to probe the piezoelectric response of samples.<sup>7</sup> The strain was caused by an ac electric field with piezoelectric coefficient  $d_{33}$  defined by:

$$d_{33}^T = \left( \frac{\partial S_3}{\partial E_3} \right)_T \quad (2.3)$$

where  $S$  is the strain induced by the field  $E$ , and the stress  $T$  is constant. The  $x_3$  axis is the direction of spontaneous polarization, which is perpendicular to the film surface. The film is clamped on a rigid substrate and can only expand or contract in the direction perpendicular to the surface and parallel to the applied field. Thus, the conditions are not truly stress free. Therefore, the measured piezoelectric response represents an effective coefficient.

In the measurements a modified Mach-Zehnder interferometer combined with an ac lock-in technique was used, as shown in fig. 2.10. A He-Ne laser beam with wavelength 632 nm was focused to a 0.5 mm diameter on the sample. The bottom of the sample is glued to the sample holder while the top is free to move so that any changes in the sample thickness produce a shift  $\Delta\phi$  in the optical phase difference  $\phi_0$  between the signal and reference beam. A Babinet-Soleil compensator was used as a variable thickness plate to adjust the phase difference to the most sensitive point ( $\phi_0 = \pm \frac{\pi}{2}$ ). A function generator provided both a dc and ac signal to the

sample. The dc voltage served as the field for polarizing the ferroelectric, while the small sinusoidal ac voltage acted as the piezoelectric driving field. The interferometer output was proportional to the effective piezoelectric coefficient. The induced phase change is given by

$$\Delta\phi = \frac{4\pi}{\lambda} \cos\theta d_{33}(\text{eff})V_{ac} \quad (2.4)$$

where  $\lambda$  is the wavelength of the He-Ne laser,  $\theta = 45^\circ$  is the incidence angle of the beam relative to the normal of the sample surface, the oscillation signal  $V_{ac}$  is kept small relative to the coercive voltage of the film and the refractive index of air is taken as 1. This phase change causes an intensity change in the interferometer:

$$\Delta I = \mp 2\sqrt{I_1 I_2} \sin(\Delta\phi) \approx \mp \sqrt{I_1 I_2} \Delta\phi \quad (2.5)$$

when  $\Delta\phi \ll 1$  and  $\phi_0 = \pm \frac{\pi}{2}$  and  $I_1$  and  $I_2$  are the intensities of the sample and reference beams. The intensity modulation  $\Delta I$  was measured by the detector in combination with a lock-in amplifier referenced to the modulation frequency of the function generator. The whole apparatus was mounted on an optical table and sealed in a box to reduce mechanical and acoustical disturbances.

For this study, the ac test signal was kept at a small amplitude of 0.5 V (about 10% of the coercive voltage of the test sample) with an oscillation frequency of 1 khz. For comparison, a pyroelectric signal hysteresis loop was measured on a 20 ML sample prior to the piezoelectric measurements. It's important to note that in the piezoelectric technique for monitoring the polarization state of the ferroelectric, the piezoelectric signal and applied voltage are recorded simultaneously. Therefore, this method probes the dynamic state of polarization while the



pyroelectric signal is proportional to the remanent polarization. Also, the pyroelectric technique can be susceptible to transient currents, while the piezoelectric technique is truly noninvasive. Fig. 2.11 shows the pyroelectric signal and piezoelectric coefficient for the same 20 ML sample. The two loops match remarkably well and yield nearly the same coercive voltage. There are a few differences: 1) the piezoelectric measurement is dynamic, therefore there is a significant difference between the saturated value and that measured at zero bias and 2) the signal to noise ratio is considerably less in the piezoelectric case and thus the loop does not appear as smooth as the pyroelectric loop. It may be important to note that the measured value of the piezoelectric coefficient for this film is considerably less than previous measurements for LB films. The previously reported value was 20 pm/V for a 15 nm film that was fabricated in Moscow. Those films are reported to be thinner<sup>6</sup> ( $\sim 0.5$  nm per LB deposition step) and this discrepancy in the piezoelectric data also suggests that films originating in Moscow may be considerably more crystalline.

## References

1. M. Bai, Ph.D., University of Nebraska, 2002.
2. K. Omote, H. Ohigashi and K. Koga, *J. Appl. Phys.* **81**, 2760 (1996).
3. C. B. Sawyer and C. H. Tower, *Phys. Rev.* **35**, 269 (1930).
4. G. Zhu, Z. Zeng, L. Zhang and X. Yan, *Appl. Phys. Lett.* **89**, 102905 (2006).
5. A. G. Chenoweth, *J. Appl. Phys.* **27**, 78 (1956).
6. A. V. Bune, S. Ducharme, V. Fridkin, N. Petukhova, A. Sorokin, K. Verkhovskaya, S. Yudin and A. Zlatkin, *Appl. Phys. Lett.* **67**, 3975 (1995).
7. A. V. Bune, C. Zhu, S. Ducharme, L. M. Blinov, V. M. Fridkin, S. P. Palto, N. G. Petukhova and S. G. Yudin, *J. Appl. Phys.* **85**, 7869 (1999).
8. M. E. Lines and A. M. Glass, *Principles and Applications of Ferroelectrics and Related Materials* (Clarendon, Oxford, 1977)

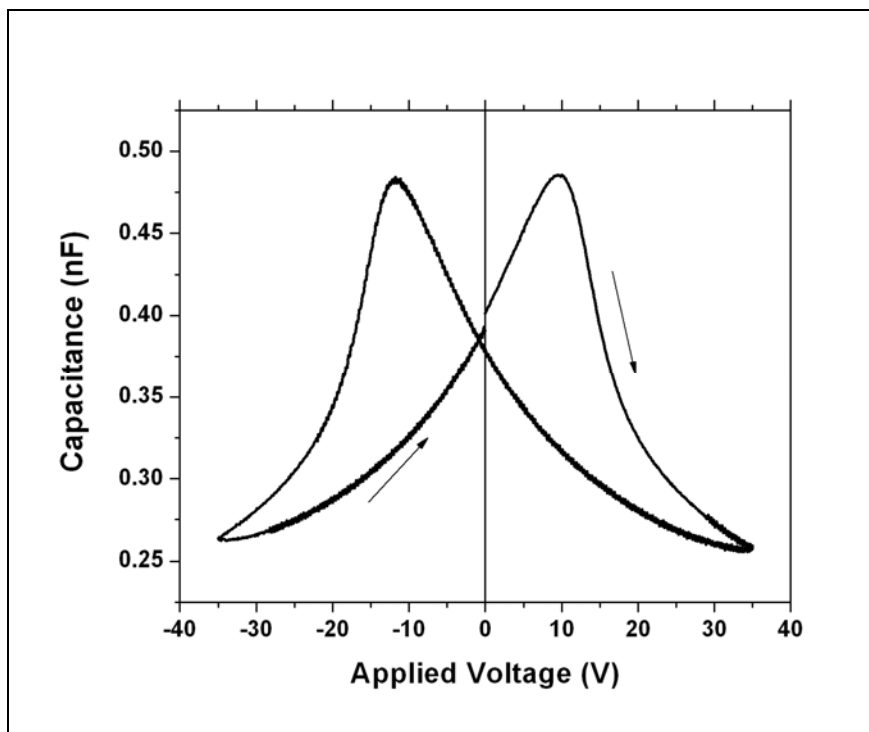


Fig. 2.1 Capacitance Voltage 'butterfly' loop for a 100 ML copolymer film.

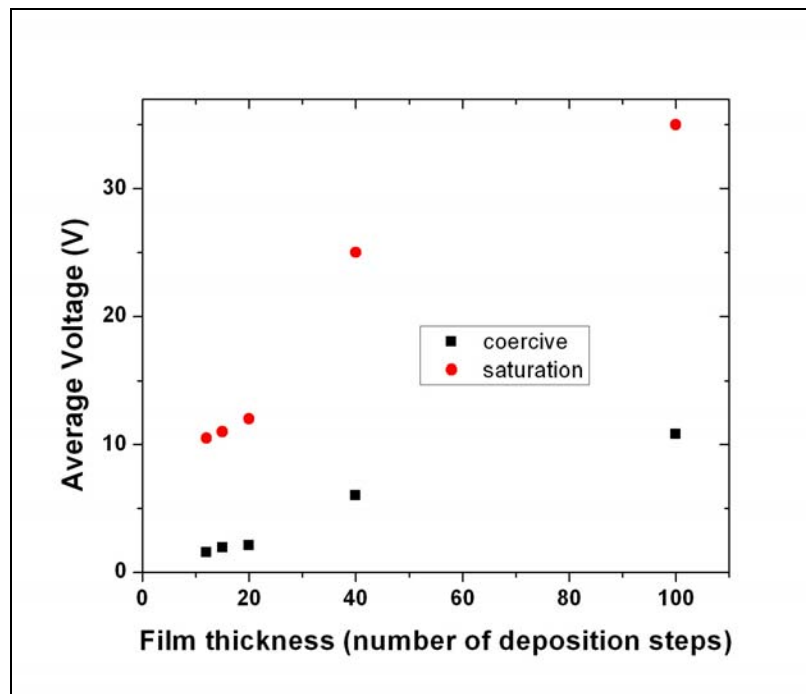


Fig. 2.2 Average values for coercive and saturation voltages for films of varying thicknesses.

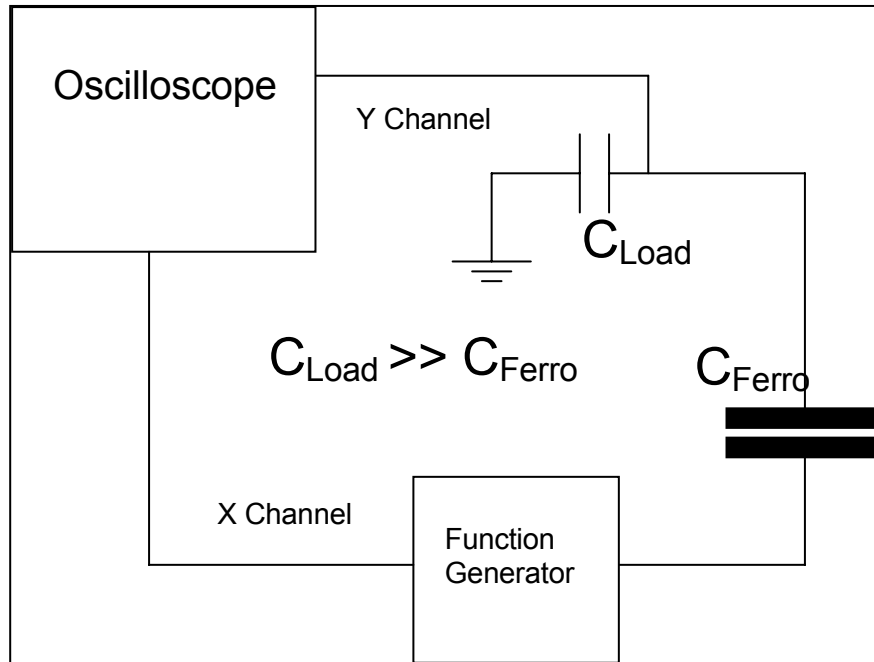


Fig. 2.3 Schematic of the Sawyer Tower circuit used to measure polarization hysteresis.

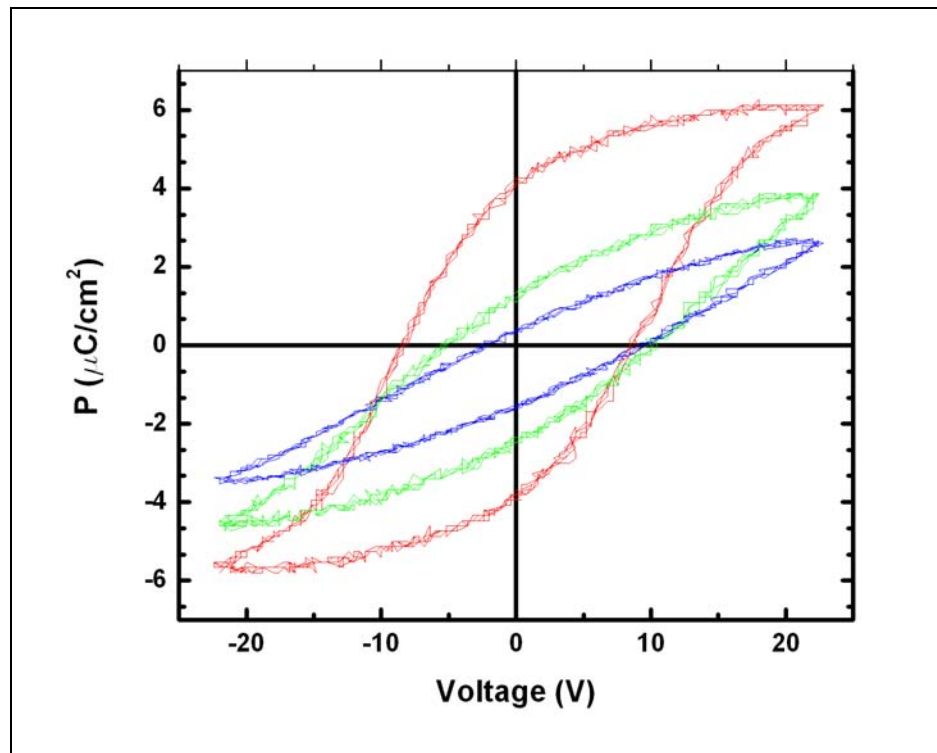


Fig. 2.2 Sawyer Tower loops for a 30 ML film with an applied triangle wave at frequencies of 10, 100 and 1000 hz.

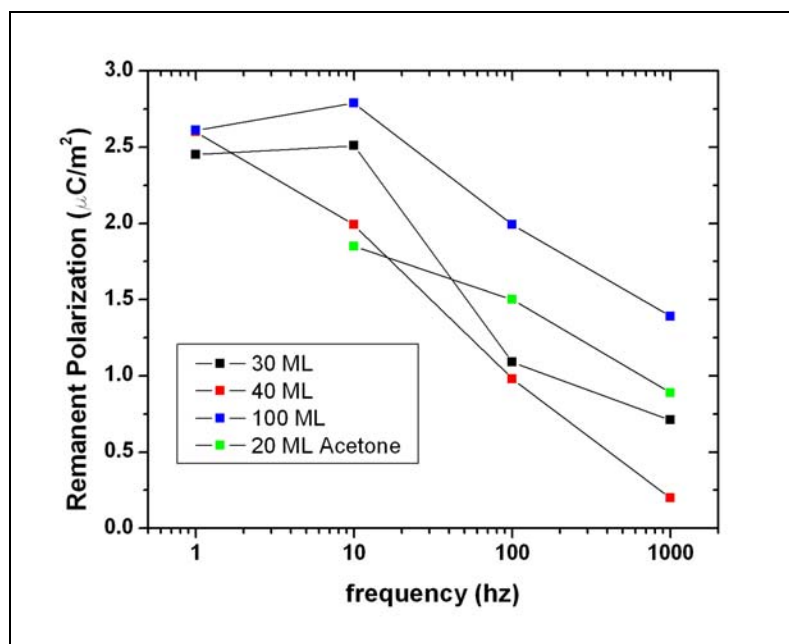


Fig. 2.5 Average remanent polarization for films of various thicknesses measured at a number of different waveform frequencies.

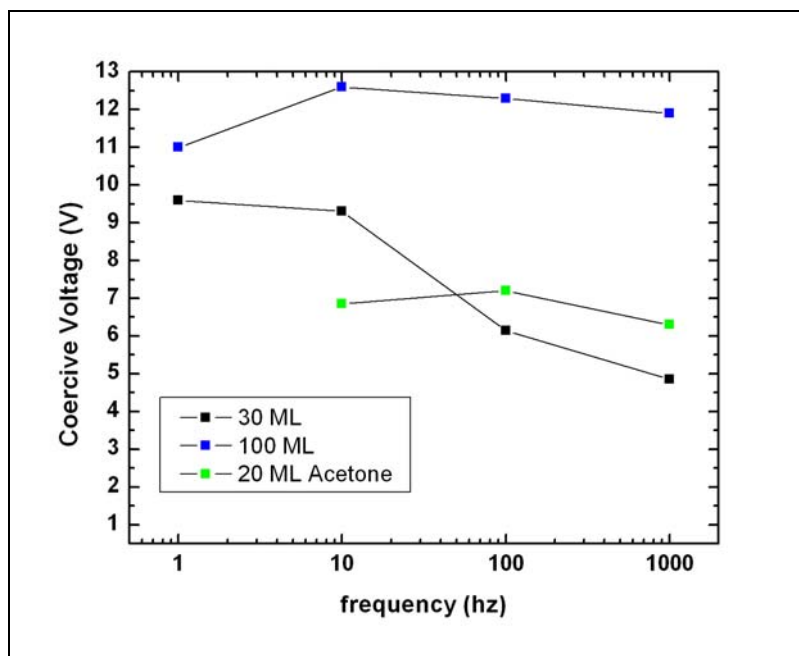


Fig. 2.6 Average coercive voltages for films of various thicknesses measured at a number of different waveform frequencies.

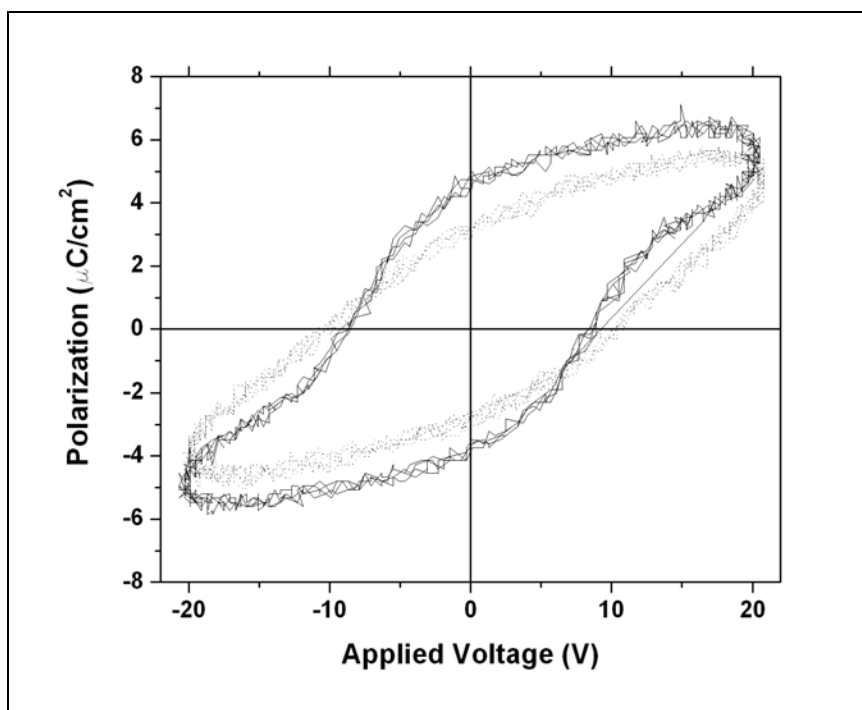


Fig. 2.7 Sawyer Tower polarization loops for a 20 ML film before and after 100 thousand cycles.

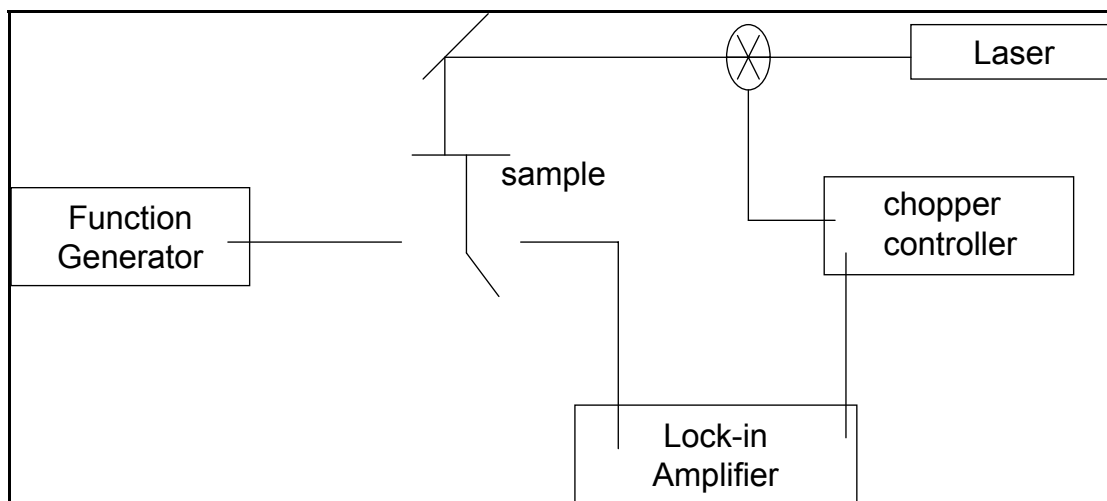


Fig. 2.8 Schematic of the experimental set-up for making pyroelectric signal measurements.

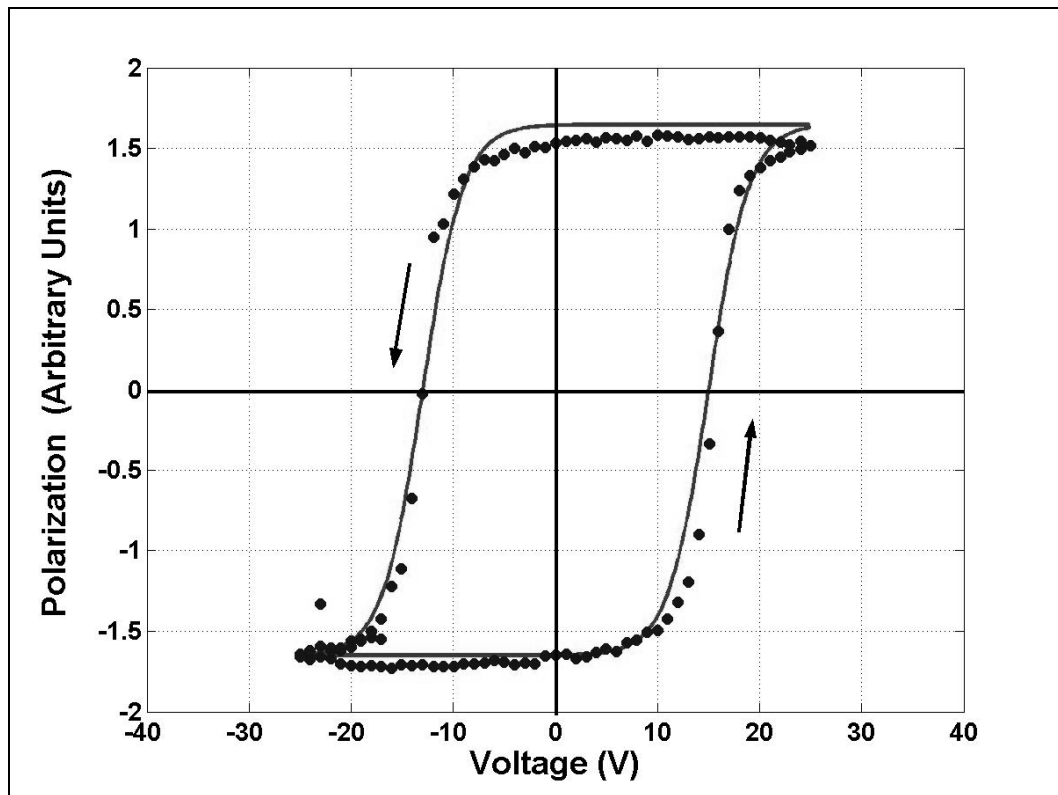


Fig. 2.9 Hysteresis in the pyroelectric signal for a 100 ML copolymer film.

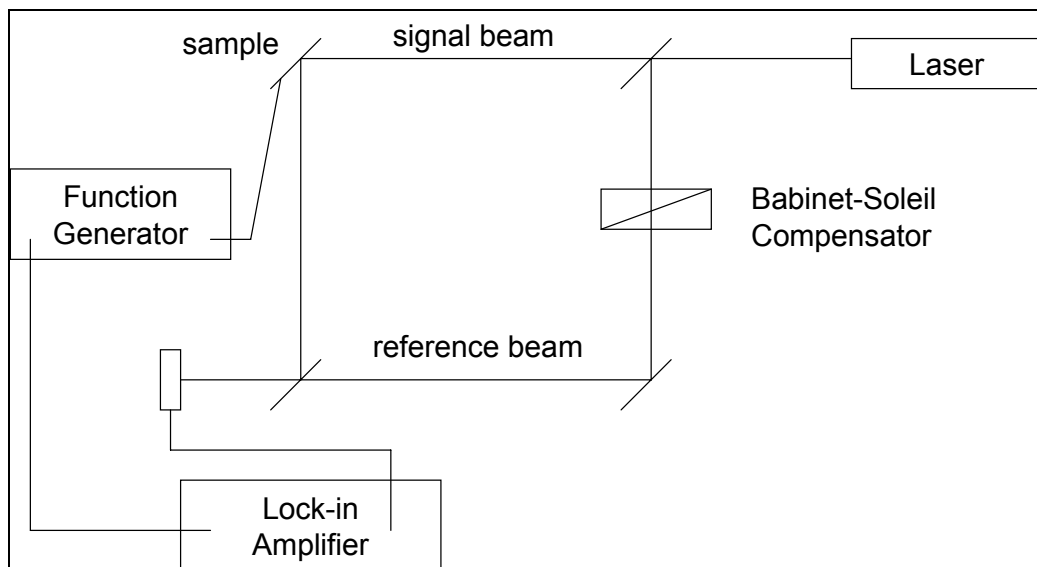


Fig. 2.10 Schematic of the experimental set-up for making inverse piezoelectric signal measurements.

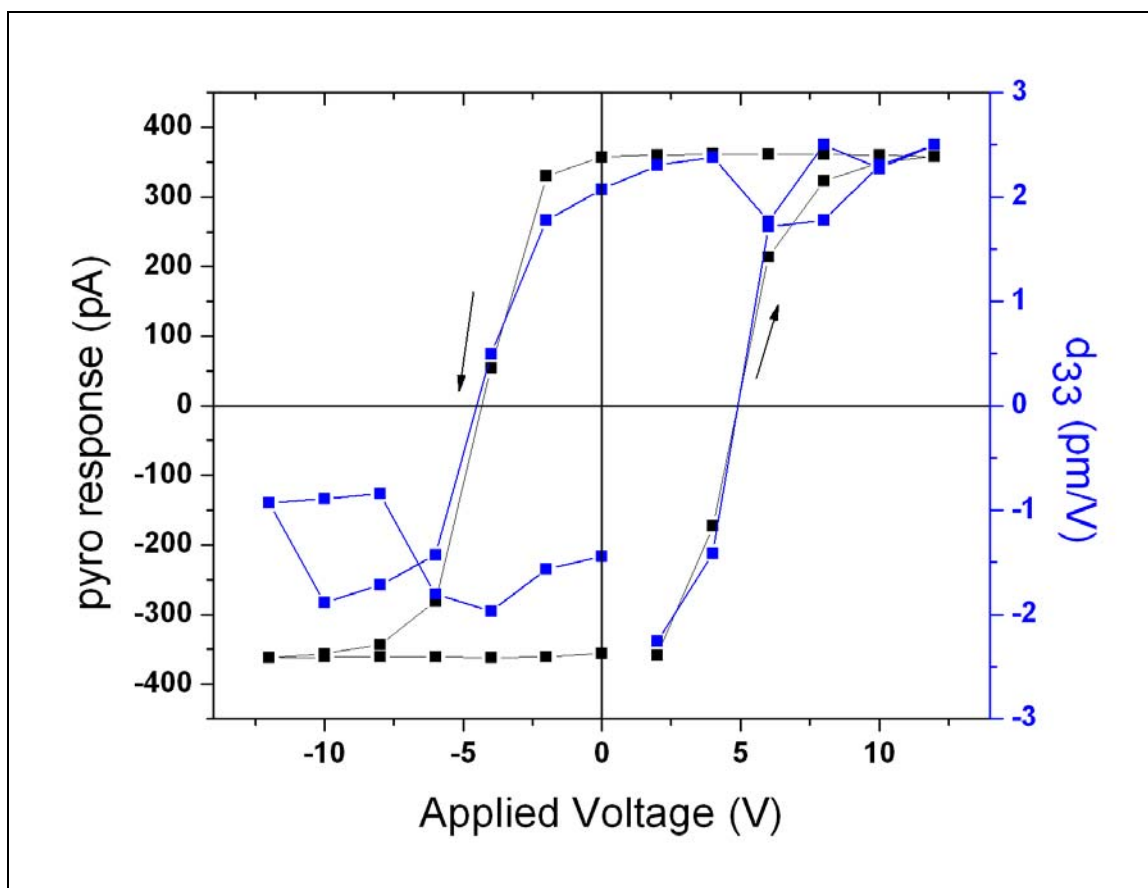


Fig. 2.11 Plot of both pyroelectric and piezoelectric hysteresis for a 20 ML film.



## INTRODUCTION TO THE METAL-FERROELECTRIC-INSULATOR-SEMICONDUCTOR (MFIS) FIELD EFFECT TRANSISTOR

Demand for nonvolatile memory devices has been growing as many electronic products become more portable and more wireless.<sup>1</sup> Ferroelectric thin films are promising for nonvolatile memory applications, such as 1T-1C ferroelectric random access memory (FRAM) and metal-ferroelectric-insulator-semiconductor field effect transistors (MFIS-FETs).<sup>2</sup> Ferroelectric memories have attracted much attention recently because of the lower writing voltage and faster switching speed than those of flash memory.<sup>3</sup> The FET type memory has a number of specific advantages, including nondestructive readout and a scalable single device structure.<sup>4</sup> It has been noted that the MFSFET will be the mainstream of high density (tens of MBit to GBit) nonvolatile RAM in the future.<sup>5</sup>

The MFIS-FET (Fig. 3.1) is based on the classical metal-oxide-semiconductor FET (or MOSFET), with the gate dielectric replaced by the combination of a ferroelectric and dielectric layer, the latter aims to prevent degradation and interdiffusion.<sup>6</sup> The application of a voltage pulse to the gate sets (writes) the direction of the ferroelectric polarization. The polarization direction controls the electrical conductance of the channel under the ferroelectric and thus the drain current of the FET. The binary level of the channel conductance can be used to define two logic states, and can be sensed (read) without affecting the ferroelectric polarization.<sup>1</sup> The main challenge in realizing a FET-type memory is to obtain a reliable ferroelectric/semiconductor interface because the interface diffusion and reaction increase the interface trap density and seriously degrade the memory characteristics.<sup>7</sup> A high  $k$  insulating layer is attractive because proportionally larger voltage can be applied across the ferroelectric

layer.<sup>4</sup> Although the concept of the ferroelectric FET (FeFET) is attractive and was first introduced back in 1957,<sup>8</sup> some problems still need to be solved to allow industrial applications since the data retention time in this structure is generally very short due to the generation of the depolarization field in the ferroelectric.<sup>9</sup>

## I. OPERATING MODES OF THE MFIS CAPACITOR

The characteristics of the gate capacitor of a FeFET can yield deep insight into the characteristics of the device. For simplicity, this treatment will be limited to a p-type silicon substrate. Such a structure is called an n-MFIS capacitor because a large positive gate bias introduces a minority n channel at the silicon interface.

### A. Modes of Operation

1. Flatband- When the gate voltage is equal to the flatband voltage,  $V_G = V_{FB}$ ; the energy bands in the semiconductor are flat. There is no charge in the gate electrode or the semiconductor. The flatband voltage is given by expression (3.1) where  $\Phi_{MS}$  is the work function difference (in Volts) between the metal gate electrode and the semiconductor.

$$V_{FB} = \Phi_{MS} - \frac{Q'_{ins}}{C_{ins}} \quad (3.1)$$

Any trapped charges that are present in the capacitor stack are denoted by  $Q'_{ins}$ . It is important to note that there are normally two gate voltages that meet the flatband condition, due to the polarization hysteresis of the ferroelectric layer. The exception occurs when the capacitance-voltage

characteristics are measured for a pristine MFIS sample at a low enough gate voltage to show the shape of the curve without providing hysteresis.

2. Accumulation- When  $V_G < V_{FB}$ , the capacitor is in accumulation and positive majority carriers accumulate at the silicon surface. The energy bands are bent, but this band-bending occurs at the interface at a small depth. The voltage drop is almost entirely across the gate insulators and thus the device capacitance is equivalent to that of the insulating stack,  $C_{ACC}=C_{INS}$ .
3. Depletion- When the gate bias lies between the flatband and threshold voltages,  $V_{FB} < V_G < V_{TH}$ , the device is in depletion mode. Now, the majority carriers are drawn away from the silicon surface leaving behind negatively charged donor ions. This region, which is lacking free carriers, is called the depletion layer of the MFIS device. As  $V_G$  is increased further, more donor atoms are ionized, increasing the depletion layer thickness. The dependence of this thickness on the silicon surface potential can be approximated by treating the device as a one-sided p-n junction.<sup>10</sup>
4. Inversion- When  $V_G > V_{TH}$ , the semiconductor is in inversion and a thin conducting channel of electrons builds at the surface. At the onset of inversion,  $V_G = V_{TH}$ , the silicon surface becomes just as n-type as the bulk is p-type. This condition occurs when the surface potential  $\phi_s$  equals twice the quasi-Fermi potential,  $\phi_F = \frac{kT}{e} \ln \frac{N_A}{n_i}$ . It is again important to note that the inversion condition is met twice per cycle due to polarization hysteresis in the

ferroelectric. Inversion mode is often referred to as the ‘on state’, because in this state, the resistance between the source and drain of a FET is low compared to the other states.

## B. Small-Signal Capacitance Voltage Characteristics of the MOS Capacitor<sup>11</sup>

For simplicity and completeness, this section will derive the relationship between device capacitance and silicon surface potential for a basic MOS (metal-oxide-semiconductor) device. Then, the following section will build on these results to demonstrate the effects of the ferroelectric film within an MFIS capacitor. Readers who are familiar with the physics of MOS capacitors may want to skip ahead to that section. The differential or small-signal capacitance of an MOS device is defined by

$C = \frac{dQ}{dV_G}$ . Any change in the gate voltage will result in potential changes across the oxide layer and the silicon surface:

$$\Delta V_G = \Delta V_{ox} + \Delta \phi_s \quad (3.2)$$

Therefore, the small signal capacitance expression for the MOS capacitor can be rewritten as (replacing the small changes with differentials):

$$\frac{1}{C} = \frac{dV_{ox}}{dQ_G} + \frac{d\phi_s}{(-dQ_s)} \quad (3.3)$$

The previous expression makes use of the condition of charge neutrality (the change in charge density at the silicon surface,  $dQ_s$ , must be equal and opposite to the charge

density change in the gate metal,  $dQ_G$ . The above expression is equivalent to the combination of two capacitors in series:

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_s(\phi_s)} \quad (3.4)$$

Generally, the oxide is treated as a linear capacitor;  $C_{ox}$  is independent of  $\Delta V_{ox}$ .

Therefore, eqn. (3.4) provides the device small signal capacitance as a function of the silicon surface potential  $\phi_s$ . This expression can be used when the silicon charge density is known as a function of surface potential.

### **Poisson's equation for extrinsic silicon**

The one-dimensional Poisson's equation relating potential,  $\phi(y)$  and charge density in the silicon,  $\rho(y)$ , is given by:

$$\frac{d^2\phi(y)}{dy^2} = -\frac{\rho(y)}{\epsilon_s} \quad (3.5)$$

Where  $y$  represents the depth within the silicon material measured from the surface and  $\epsilon_s$  is the permittivity of the semiconductor.

There are four quantities that make up the charge density within an extrinsic semiconductor. These are the densities of the free electrons  $n$ , holes  $p$ , ionized donor atoms  $N_D$ , and ionized acceptor atoms  $N_A$ . The number of donor atoms in a p-type material is usually negligible, thus the total charge density is given by:

$$\rho(y) = q_e(p(y) - n(y) + N_A) \quad (3.6)$$

The concentrations  $p(y)$  and  $n(y)$  are governed by Maxwell-Boltzmann statistics (provided that the silicon is nondegenerate):

$$p(y) = p_0 e^{\frac{-\varphi(y)}{\phi_i}} \quad (3.7a)$$

$$n(y) = n_0 e^{\frac{\varphi(y)}{\phi_i}} \quad (3.7b)$$

$p_0$  and  $n_0$  represent the bulk hole and electron concentrations respectively. Deep in the bulk the charge density is zero, therefore

$$p_0 - n_0 = N_A \quad (3.8)$$

and eqn. (3.5) becomes:

$$\frac{d^2\varphi}{dy^2} = -\frac{q}{\epsilon_s} \left[ p_0 \left( e^{\frac{-\varphi}{\phi_i}} - 1 \right) - n_0 \left( e^{\frac{\varphi}{\phi_i}} - 1 \right) \right] \quad (3.9)$$

This expression can be further simplified if a few approximations are made. In the bulk of doped p-silicon, the concentrations of acceptor atoms are commonly several order of magnitude higher than the silicon intrinsic carrier concentration. Therefore, the free hole concentration in the bulk ( $p_0$ ) may be approximated by  $N_A$ . The other useful assumption is that the pn product of silicon is not affected by doping.

$$p_0 \approx N_A \quad (3.10a)$$

$$n_0 \approx \frac{p_0^2}{N_A} \quad (3.10b)$$

Inserting expressions (3.10a) and (3.10b) into equation (3.9) yields the following result:

$$\frac{d^2\varphi}{dy^2} = \frac{-qN_A}{\epsilon_s} \left[ e^{\frac{2\phi_F}{\phi_t}} \left( e^{\frac{-\varphi(y)}{\phi_t}} - 1 \right) - \left( e^{\frac{\varphi(y)}{\phi_t}} - 1 \right) \right] \quad (3.11)$$

If both sides of this expression are multiplied by the quantity  $2\left(\frac{d\varphi}{dy}\right)$ , the equation

can be readily solved. The left hand side is then recognized as  $\left(\frac{d}{dy}\right)\left(\frac{d\varphi}{dy}\right)^2$  and the

right hand side can be integrated, using a dummy variable, from a point deep in the

bulk (where  $\varphi = 0$ ) to a point  $y$ . Only the result is given here:

$$E(y) = -\frac{d\varphi}{dy} = \pm \frac{\sqrt{2q_e N_A \epsilon_s}}{\epsilon_s} \left[ \sqrt{e^{\frac{2\phi_F}{\phi_t}} \left( -\phi_t + \varphi + \phi_t e^{\frac{-\varphi}{\phi_t}} \right) - \phi_t - \varphi + \phi_t e^{\frac{\varphi}{\phi_t}}} \right] \quad (3.12)$$

The positive sign is used when  $\varphi > 0$  and the negative sign is physically valid when

$\varphi < 0$ .

The application of Gauss' law from the surface to a point deep within the bulk (where the field is zero) relates the electric field at the surface to the net charge per unit area

beneath the oxide layer,  $Q_s$ :

$$-E_{SURFACE} = \frac{Q_s}{\epsilon_s} \quad (3.13)$$

Now equations 3.12 and 3.13, evaluated at the surface ( $y=0$ ) can be combined to relate the silicon surface charge density to the surface potential:

$$\sigma_s = \mp \sqrt{2q_e N_A \epsilon_s} \left[ \sqrt{e^{\frac{2\phi_F}{\phi_t}} \left( -\phi_t + \phi_s + \phi_t e^{\frac{-\phi_s}{\phi_t}} \right) - \phi_t - \phi_s + \phi_t e^{\frac{\phi_s}{\phi_t}}} \right] \quad (3.14)$$

The differential capacitance of the semiconductor,  $C_s(\phi_s)$  is readily calculated by differentiating (3.14):

$$C_s = -\frac{d\sigma_s}{d\phi_s} = \pm \sqrt{2q_e N_A \epsilon_s} \frac{-e^{\frac{2\phi_F}{\phi_t}} \left( e^{\frac{-\phi_s}{\phi_t}} - 1 \right) + e^{\frac{\phi_s}{\phi_t}} - 1}{2 \sqrt{e^{\frac{2\phi_F}{\phi_t}} \left( -\phi_t + \phi_s + \phi_t e^{\frac{-\phi_s}{\phi_t}} \right) - \phi_t - \phi_s + \phi_t e^{\frac{\phi_s}{\phi_t}}}} \quad (3.15)$$

This equation used with equation (3.4) gives the small signal response of the semiconductor for all values of its surface potential,  $\phi_s$ .

The important aspects of a typical device capacitance plot is shown by the example given in fig. 3.2. This particular modeled sample exhibits accumulation mode for all gate voltages below 0 bias. In accumulation, a differential change in the AC signal causes a small change in the density of majority carriers at the silicon surface. In this case, the capacitance of the silicon is large compared to that of the oxide layer.

Therefore the series capacitance in this region equals the linear capacitance of the oxide layer.



For relatively small positive voltages associated with the depletion mode of operation (between 0 V and  $V_{th}$ ), majority carriers are driven away from the silicon surface, leaving ionized acceptor atoms behind. In this mode, a small change in the sinusoidal signal corresponds to a differential change in the thickness of the depletion layer. As the depletion layer grows with increasing bias, the capacitance decreases until the depletion layer thickness reaches a maximum at the threshold voltage,  $V_{th}$ . The threshold voltage for this example is approximately +1.3 V.

When a fairly large positive voltage beyond  $V_{th}$  is applied to the device, electrons are drawn to the surface of the silicon. Thus, in this inversion mode, the device response is determined by the majority carriers and the small signal capacitance reverts to that of the oxide layer.

The value of the flatband capacitance is particularly useful for determining the amount of effective trapped charge in the insulating layers, as discussed near the end of this chapter. Due to the charge variations in the semiconductor, the small signal capacitance at flatband is slightly less than the value in accumulation:<sup>12</sup>

$$C_{FB} = \frac{1}{\frac{1}{C_{ACC}} + \frac{L_D}{\epsilon_S}} \quad (3.16)$$

where  $L_D = \sqrt{\frac{\epsilon_S V_t}{eN_a}}$  is the Debye length.

### Frequency dependence

The previous equations defining the characteristics of the MOS structure are only valid when equilibrium is established in the semiconductor. That is, the period of the AC signal must be large in comparison to the typical response time of the silicon.

In accumulation and depletion, majority carriers govern the response time of the device. The electrons will follow the small AC signal as long as the period of oscillation is much longer than the dielectric response time. For highly doped n type silicon, this quantity is on the order of a picosecond. Thus, the assumption of equilibrium for these modes is certainly valid for all signal frequencies below 1 GHz.

As was mentioned above in the description of the inversion mode of operation, the much slower minority carrier response defines the boundary of quasistatic processes in inversion. There are two main processes through which minority carriers arrive at the silicon surface: 1) generation and recombination of minority carriers in the depletion layer (dominant process near room temperature) and 2) generation of minority carriers at the back contact followed by the diffusion through the bulk material and then drift through the depletion layer (dominant process at high temperatures). In either case, a frequency dependence of the C-V curves arises when the minority carriers lag behind the small driving signal. For high small-signal frequencies, the capacitance will remain low in the strong inversion regime. This lag produces an energy loss in the system evident in a rise in the AC conductance. The RC time constant related to the loss yields a means to measuring the minority carrier response time, which typically lies within the range of 0.01 to 1 sec. The minority response can be quickened by illuminating the sample with light of wavelengths below 1 micron to generate electron hole pairs more quickly than thermal excitation does.

### C. Modeling the MFIS Capacitor

The silicon physics of a MOS device is independent of the dielectric structure that exists above the surface of the silicon. The layers above the silicon simply determine the relationship between the silicon surface potential and the applied gate bias. The same is true for the MFIS structure except that this relationship will depend on the electrical history. Miller et al.<sup>13-15</sup> provided a successful model for the characteristics of the MFIS structure by combining the charge-sheet model of the previous section with a solution to Maxwell's equation that uses a tanh function representation of the ferroelectric polarization hysteresis. Their theoretical results provide insight into the effects of material parameters on the properties of the device. In this section, their theory is summarized and then used to model a specific polymer based MFIS capacitor.

The electrostatic equations for the capacitor structure are derived starting with Maxwell's equation:

$$\Delta \cdot D = \rho \quad (3.17)$$

Where  $D$ , the displacement vector is given by (vector quantities are taken to be positive in the direction pointing down from the top electrode:

$$D = \epsilon_0 E + P_{total} \quad (3.18)$$

The total polarization  $P_{total}$  is the sum of the linear contribution and the contribution from switching dipoles, thus

$$D = \epsilon_0 E + \epsilon_0 \chi E + P_D = \epsilon_0 \epsilon E + P_D \quad (3.19)$$

where  $P_D$  is the contribution to the polarization due to switching dipoles and it is a function of the electric field in the ferroelectric layer as well as the electrical history.

Combining (3.17) and (3.19) together with the definition  $E = -\nabla\phi$ :

$$V_{GB} = \phi_S - \frac{\sigma_S}{C_{STACK}} - \frac{P_D d_f}{\epsilon_0 \epsilon_f} + \Phi_{MS} \quad (3.20)$$

where

$$C_{STACK} = \left( \frac{d_{ins}}{\epsilon_0 \epsilon_{ins}} + \frac{d_f}{\epsilon_0 \epsilon_f} \right)^{-1} \quad (3.21)$$

and the electric field of the ferroelectric is given by:

$$E_f = - \left( \frac{\sigma_S + P_D}{\epsilon_0 \epsilon_f} \right) \quad (3.22)$$

An expression for the silicon surface charge density as a function of surface potential was derived in the previous section, equation (3.14).

#### D. Operating Voltage

The gate voltage required to saturate the ferroelectric film can be determined by inserting the saturation values,  $P_{SAT}$  and  $E_{SAT}$ , into equation (3.20) under the condition of strong inversion  $\phi_S = 2\phi_F$  (saturation with inversion will require a greater voltage than under the accumulation condition because of the potential drop across the depletion layer).<sup>16</sup>

Substituting (3.22) into (3.20) and using saturation values:

$$V_{GB}^{SAT} = 2\phi_F + \frac{\epsilon_0 \epsilon_F E_{SAT}}{C_{STACK}} + \frac{P_{SAT}}{C_{ins}} + \Phi_{MS} \quad (3.23)$$

The relationship between coercive field and Langmuir-Blodgett copolymer film thickness has already been established.<sup>17</sup> The data show that for films thicker than 15 nm, the coercive field scaled at the -0.7 power of the thickness, indicating that switching is dominated by the nucleation mechanism. Below 15 nm, the intrinsic coercive field of 0.5 GV/m is reached. (The coercive and saturation fields can be lowered by up to a factor of 10 by changing film deposition conditions). By assuming that the field required for saturation is approximately 50% larger than these values (Fig. 3.3), the expression above was solved for several ferroelectric and buffer layer thicknesses (Fig. 3.4). In the case of the silicon oxide ( $\epsilon_{ins} = 3.9$ ) buffer layer (Fig. 3.4a), the saturation gate voltage is extremely high, even in the thinnest buffer layer case of 10 nm. Furthermore, the  $P_{SAT}$  term in eqn. 3.23 dominates for all ferroelectric thicknesses due to the low dielectric constant of the insulating layer and as a result, there is little variation of the saturation voltage for a given oxide thickness.

When hafnium oxide ( $\epsilon_{ins} \approx 25$ ) is used as the buffer layer (Fig. 3.4b), the saturation voltage is reduced significantly. For each buffer layer thickness shown, a relative minimum in the saturation voltage appears at a ferroelectric thickness of 30 nm. Since Langmuir-Blodgett copolymer films thinner than 15 nm are often less reliable in terms of dielectric loss and switch more slowly, this study will focus on the film thicknesses near this 30 nm minimum.

## E. Dipole Polarization

This model includes a theoretical approximation for the ferroelectric polarization-electric field (P-E) hysteresis loop based on the tanh function. The results are simply stated here.

The saturated polarization hysteresis loop is defined by the following expression:<sup>13</sup>

$$P_{SAT}^+(E) = P_s \tanh\left[\frac{(E - E_c)}{2\delta}\right] \quad (3.24)$$

where

$$\delta = E_c \left[ \ln \left( \frac{1 + \frac{P_r}{P_s}}{1 - \frac{P_r}{P_s}} \right) \right]^{-1} \quad (3.25)$$

and the + superscript signifies the section of the loop where the field is increasing. For the section where the field is decreasing, the polarization is given by:

$$P_{SAT}^- = -P_{SAT}^+(-E) \quad (3.26)$$

The derivative of the polarization, whether or not the polarization lies on or within the saturated hysteresis loop, is given by:

$$\frac{dP_D}{dE} = \Gamma \frac{dP_{SAT}}{dE} \quad (3.27)$$

and

$$\Gamma = 1 - \tanh\left[\left(\frac{P_D - P_{SAT}}{\xi P_{SAT} - P_D}\right)^{\frac{1}{2}}\right] \quad (3.28)$$

and  $\xi = +1$  when  $\frac{dE}{dt} > 0$  and  $\xi = -1$  when  $\frac{dE}{dt} < 0$ .

An example of a modeled P-E loop using this method is shown in Fig. 3.5.

## F. Numerical Analysis Technique

To perform the integration from a set of initial conditions to a new set of conditions, a technique is needed to simultaneously solve many of the previous expressions. The approach chosen here involves selecting the  $m$ th value of  $\phi_s$ , then calculating the  $m$ th value of  $\sigma_s$  from expression 3.14. Now, the dipole polarization is written as:

$$P_d(E_m) = P_d(E_{m-1}) + (E_m - E_{m-1}) \left( \frac{d}{dE} \right) P_d(E)_{E_{m-1}} \quad (3.29)$$

By using (3.22) to eliminate  $E_m$ , (?) becomes

$$P_d(E_m) = \frac{P_d(E_{m-1}) - \left\{ \left[ \frac{\sigma_s}{\epsilon_0 \epsilon_F} \right] + E_{m-1} \right\} \left( \frac{d}{dE} \right) P_d(E)_{E_{m-1}}}{1 + \left( \frac{1}{\epsilon_0 \epsilon_F} \right) \left( \frac{d}{dE} \right) P_d(E)_{E_{m-1}}} \quad (3.30)$$

Using (3.30) together with (3.27), the  $m$ th value of the polarization is calculated. Then  $V_{GB}$  is determined using (3.20).

## G. Results

In this section, the model developed by Miller and McWhorter<sup>13</sup> will be applied to investigate a particular MFIS device involving a 35 nm thick PVDF copolymer film. All of

the parameters used are summarized in Table 3.1. Note that the ferroelectric parameters are the same as those shown in the P-E loop in Fig. 3.5.

Figure 3.6 shows the silicon surface potential for a gate voltage sweep between +15 and -15 Volts. The surface potential varies between the limits of 1.2 V in the strong inversion region to -0.4 V in accumulation mode. Throughout the voltage sweep, the potential drop across the silicon remains below 10% of the maximum applied gate voltage. The hysteresis is due to the spontaneous polarization of the ferroelectric layer.

The next figure, (3.7), shows the electric field in the ferroelectric layer as a function of the applied gate voltage for the same voltage sweep. The maximum electric field magnitude over this range was 450 MV/m (or about 2.6 times the coercive field) and it was reached in the accumulation mode. Because of the hysteresis in this field plot, a significant field exists even at zero applied bias. This field tends to switch the ferroelectric from its current polarization state and thus it is referred to as the depolarization field. It arises because the oxide or semiconductor that is in direct contact with the ferroelectric cannot provide enough charges to fully compensate for the surface charge of the polarized ferroelectric. The situation can be slightly improved by increasing the doping level in the semiconductor. The depolarization field in this case was larger after saturating the sample in strong inversion mode as opposed to accumulation (1.25 MV/m versus 1 MV/m) and therefore the sample should be slightly more stable in the negative polarization state. Since the depolarization field is not an applied field, it should decrease as ferroelectric dipoles switch until equilibrium is reestablished at zero net polarization. Thus, state retention is expected to be an issue in such a sample even after saturation. It should be noted that this model assumes that thermal equilibrium is always established within the device structure. This



may not be the case if higher ramp rates are used. In those situations, minority carriers in inversion mode may not respond to the applied signal and the remanent polarization would be even less in that state. The slow minority carrier response could also shrink the memory window under high-speed operation.

The capacitance-voltage curve (Fig. 3.8) of the MFIS structure reveals the same features as those seen in the MOS C-V curve of Fig. 3.2, but hysteresis is present due to the switchable polarization of the ferroelectric. Because of this hysteresis, the value of the flatband and threshold voltages depends on the electrical history of the sample; switching the ferroelectric polarization shifts the threshold voltage from its value in the opposite polarization state. This voltage shift is referred to as the memory window and the maximum size of this window (achieved at saturation) is the same as the width of the ferroelectric's polarization-voltage loop,  $\Delta V_{TH} = 2E_C d_F$  (measured in the MFM structure). The memory window in this case is 5 Volts after saturation. Furthermore, at zero bias one of the states remains in the strong inversion mode (high source-drain conductivity) while the other remains in accumulation. Thus, the model predicts a large, nonvolatile on/off ratio in drain current for the corresponding ferroelectric field effect transistor.

## **H. Non-Ideal Effects**

**Dielectric Breakdown-** An insulating layer is included within the metal-ferroelectric-insulator-semiconductor structure in order to prevent contamination of the silicon layer by the ferroelectric. This places limitations on the device, not only in programming voltage, but it also limits the maximum charge density in the semiconductor since the electric field

in the insulating layer must remain below its breakdown field,  $E_B$ .<sup>16</sup> The substrate charge density associated with breakdown can be defined as

$$\sigma_{CRIT} = \epsilon_{ins} E_B \quad (3.31)$$

The magnitude of the charged density induced by the saturation of the ferroelectric will be

$$\sigma_{SAT} = \epsilon_F E_{SAT} + P_{SAT} \quad (3.32)$$

Therefore, in order for the ferroelectric to achieve saturation, the ferroelectric and insulator parameters must satisfy the expression

$$\epsilon_{ins} E_B = \epsilon_F E_{SAT} + P_{SAT} \quad (3.33)$$

otherwise, the ferroelectric will undergo a “minor” hysteresis loop, reducing the size of the memory window and possibly the stability of the device.

Effective trapped charge- The presence of trapped charge  $Q_{trapped}$  in the insulating layer results in the horizontal shift of the flatband condition:

$$\Delta V_{FB} = -\frac{Q_{trapped}}{C_{stack}} \quad (3.34)$$

Thus, a positive fixed oxide charge will result in a shift in the flatband condition to more negative gate voltages.

A common source for trapped charge in all MOS devices is provided by the two broken covalent bonds (“dangling bonds”) per atom at the silicon surface, which arise due to the absence of lattice atoms above.

The procedure<sup>18</sup> for determining the contribution from the ferroelectric layer to the effective trapped charge involves first determining the corresponding trapped charge in the MOS structure, preferably from the same wafer. Then the flatband shift is measured from the C-V curve of a freshly annealed MFIS capacitor at gate voltages too low to exhibit hysteresis. The contribution of the ferroelectric to the effective trapped charge can then be calculated from the difference, taking into account the difference in device capacitance.

Surface states- Charge due to electrons occupying surface states also yields a shift in flatband voltage. However as the applied voltage is varied, the Fermi energy at the oxide-semiconductor interface changes also and affects the occupancy of the surface states.<sup>12</sup> The interface states cause the transition in the capacitance measurement to be broadened.

Mobile charge- In the case of mobile charges or defects that allow charge transport from either side of the contact, a hysteresis is observed that has either clockwise (if injection takes place from the silicon side) or counterclockwise (if the charge originates in the gate) orientation when a p-type substrate is used. In the MFIS structure, the two hysteresis curves (injection and ferroelectric) add up to a combined hysteresis that cannot be separated. In fact, the typical clockwise hysteresis from the ferroelectric can be turned counterclockwise, if a high number of oxide charges originate from the semiconductor.

Conclusion

In the case of ferroelectrics that have large coercive fields, such as PVDF and its copolymers; a large memory window is easily achieved:  $\Delta V_{TH} = 2E_C d_F$ , but this comes at the expense of large operating voltages. The copolymer's relatively low permittivity ( $\epsilon_{ferro} \approx 10$ ) results in a smaller voltage drop across the buffer layer compared to perovskite ferroelectrics, which have a much higher dielectric permittivity ( $\epsilon_{ferro} \approx 250$ ). The large remanent polarization is favorable because it can lead to higher drain-source currents in the FeFET structure. However, this also means that the ferroelectric cannot be fully polarized with low voltage operation, and less stable sub-loops are present.

Regarding the dielectric layer, it should have a high permittivity and breakdown field so that the ferroelectric can be polarized as much as possible without experiencing breakdown. Since both the properties of the ferroelectric and insulating layers prohibit saturation at low voltages in field effect devices based on ferroelectric polymers, much attention should be given to the retention times in such structures.

## References

1. P. Juan, Y. Hu, F. Chiu, and J. Y. Lee, *J. Appl. Phys.* **98**, 044103 (2005).
2. J. L. Sun, X. J. Meng, J. H. Ma, T. Lin, J. Chen, N. Dai, and J. H. Chu, *Appl. Phys. A* **81**, 389 (2005).
3. C. L. Sun, S. Y. Chen, S. B. Chen, and A. Chin, *Appl. Phys. Lett.* **80**, 1984 (2002).
4. C. Y. Chang, T. P. Juan, and J. Y. Lee, *Appl. Phys. Lett.* **88**, 072917 (2006).
5. S. B. Xiong and S. Sakai, *Appl. Phys. Lett.* **75**, 1613 (1999).
6. Y. T. Kim, C. W. Lee, D. S. Shin, and H. N. Lee, *Proc. IEEE Int. Symp. Appl. Ferroelect.*, 35 (1998).
7. A. D. Li, Y. J. Wang, Q. Y. Shao, J. B. Cheng, D. Wu, H. Q. Ling, Y. J. Bao, M. Wang, Z. G. Liu, and N. B. Ming, *Appl. Phys. A* **81**, 1273 (2005).
8. I. M. Ross, US Patent 2,791,760 (1957).
9. B. E. Park, K. Takahashi, and H. Ishiwara, *Appl. Phys. Lett.* **85**, 4448 (2004).
10. D. Neaman, *Semiconductor Physics and Devices: Basic Principles*, Irwin; Homewood, Ill. (1992).
11. Y. Tsididis, *Operation and Modeling of the MOS Transistor*, McGraw-Hill; Boston, MA (1999).
12. B. Van Zeghbroeck, *Principles of Semiconducting Devices and Heterojunctions*, Prentice Hall (2007).
13. S. L. Miller and P. J. McWhorter, *J. Appl. Phys.* **72**, 5999 (1992).
14. S. L. Miller, R. D. Nasby, J. R. Schwank, M. S. Rodgers and P. V. Dressendorfer, *J. Appl. Phys.* **68**, 6463 (1990).
15. S. L. Miller, J. R. Schwank, R. D. asby, and M. S. Rodgers, *J. Appl. Phys.* **70**, 2849 (1991).
16. J. M. Sallese and V. Meyer, *IEEE Trans. Electron Devices* **51**, 2145 (2004).
17. S. Ducharme, V. M Fridkin, A. V. Bune, S. P. Palto, L. M. Blinov, N. N. Petukhova, and S. G. Yudin, *Phys. Rev. Lett.* **84**, 175 (2000).
18. S. H. Lim, A. C. Rastogi, and S. B. Desu, *J. Appl. Phys.* **96**, 5673 (2004).

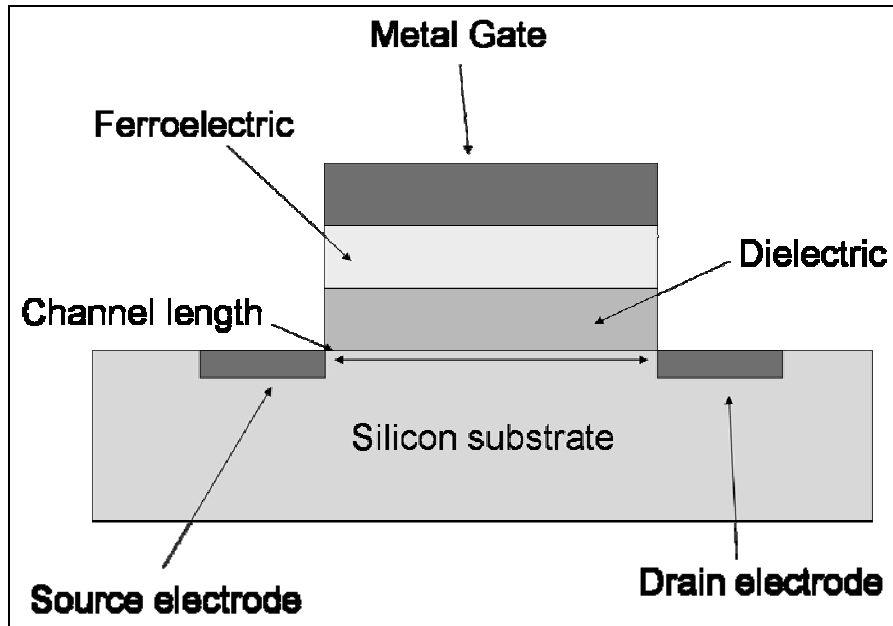


Fig. 3.1 The ferroelectric field effect transistor (FeFET).

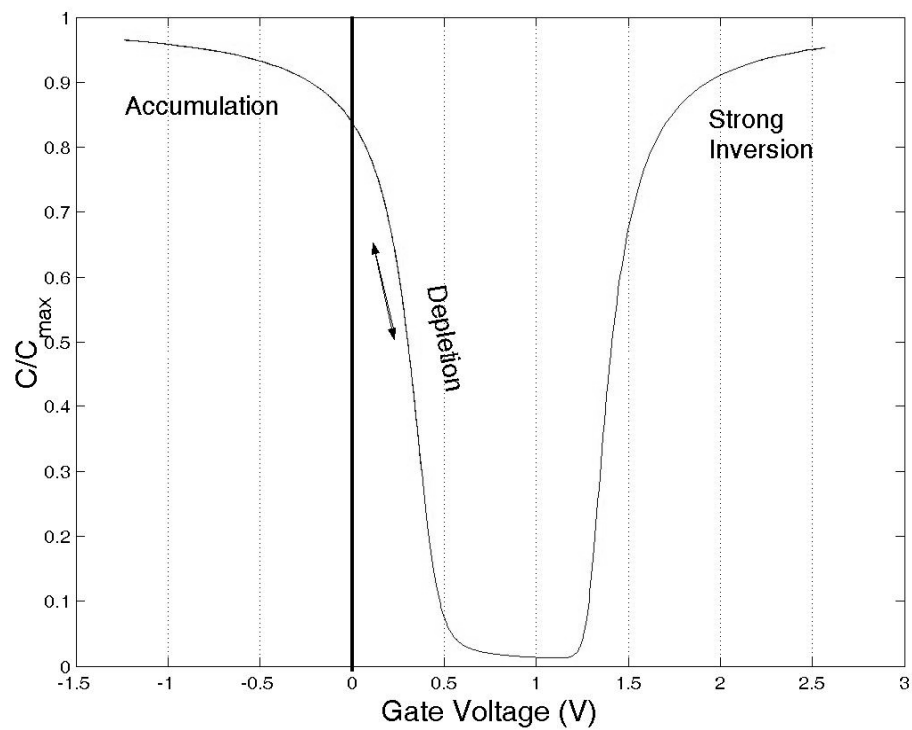


Fig. 3.2 Modeled Capacitance Voltage (C-V) characteristics for a MOS capacitor with 10 nm hafnium oxide as a dielectric.

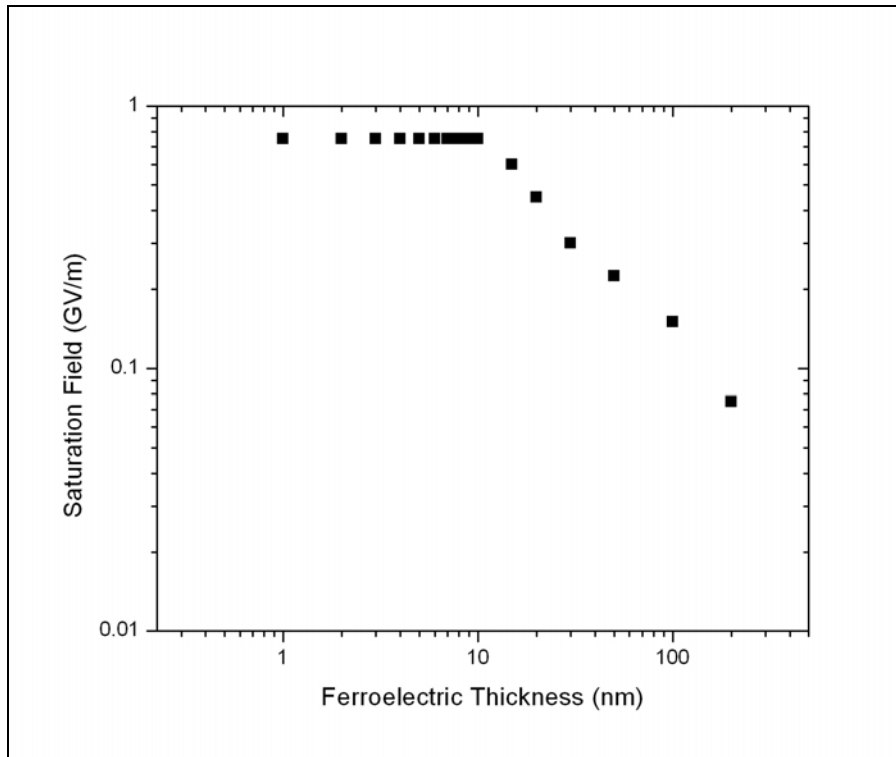


Fig. 3.3 Approximated thickness dependence of saturation field for PVDF/TrFE LB films. (derived from [17].

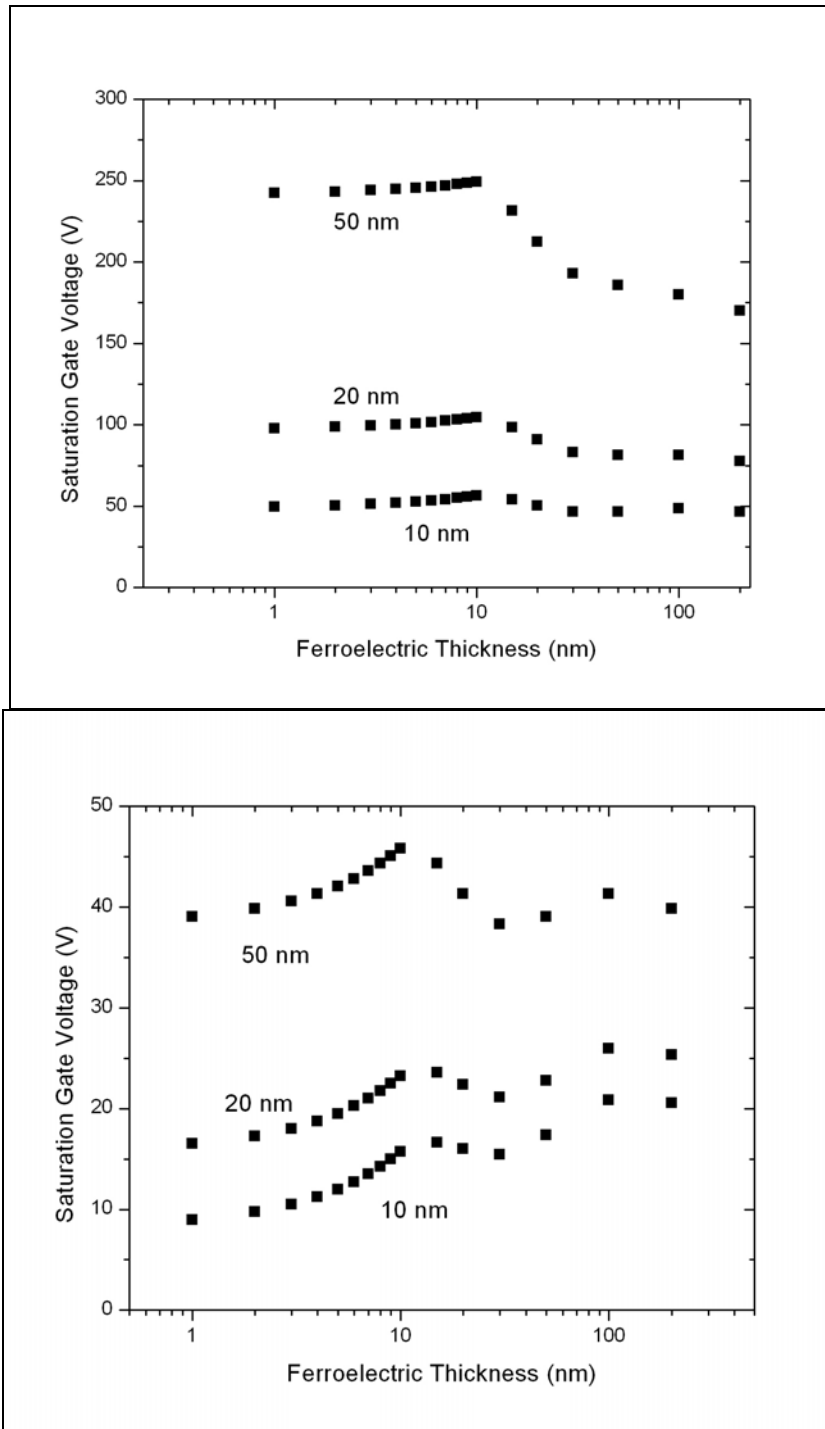


Fig. 3.4 Approximated saturation gate voltages for different thicknesses of silicon oxide (top) and hafnium oxide (bottom)



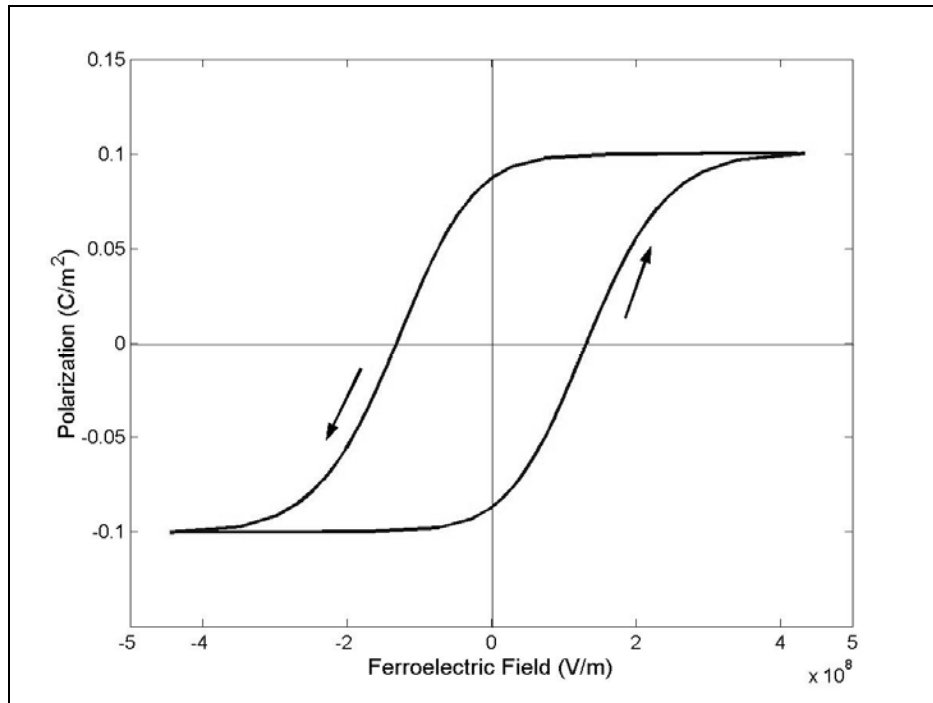


Fig. 3.5 Modeled P-E curve for a ferroelectric film.

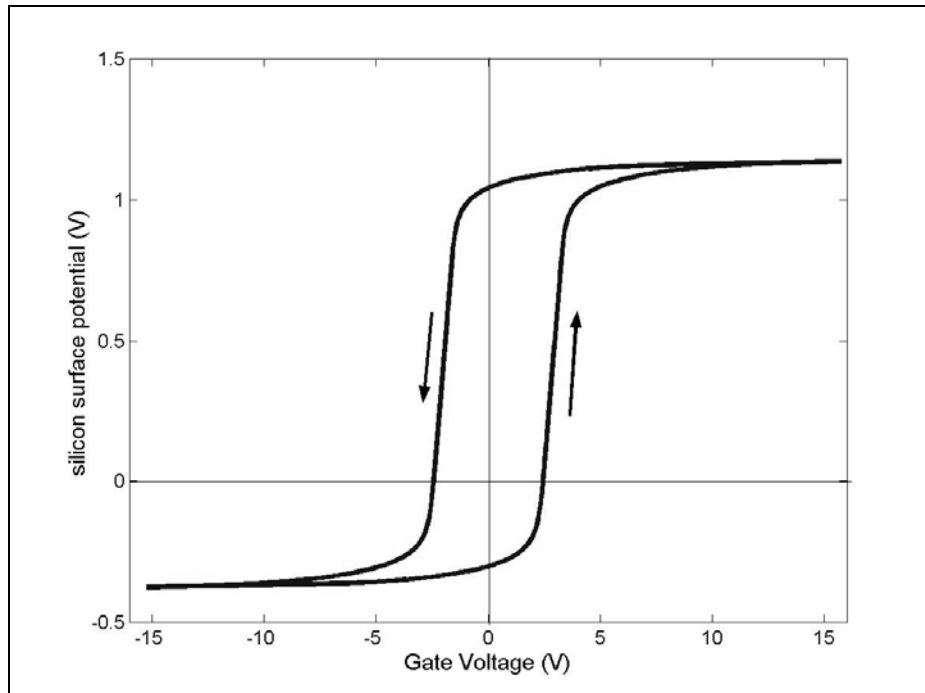


Fig. 3.6 Dependence of silicon surface potential on applied gate voltage for an MFIS.

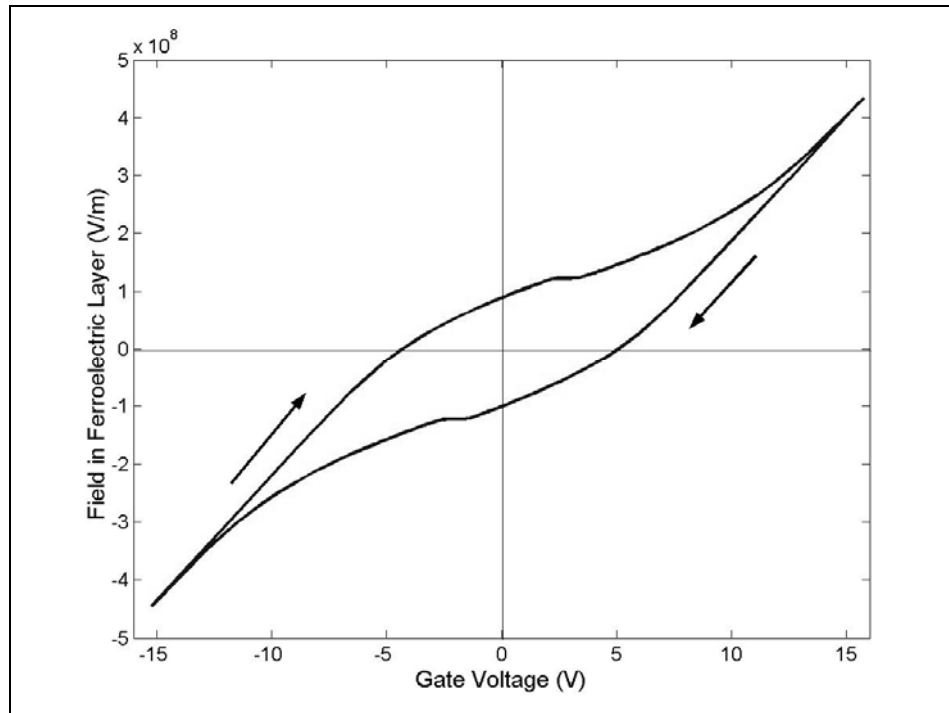


Fig. 3.7 Dependence on ferroelectric field on gate voltage.

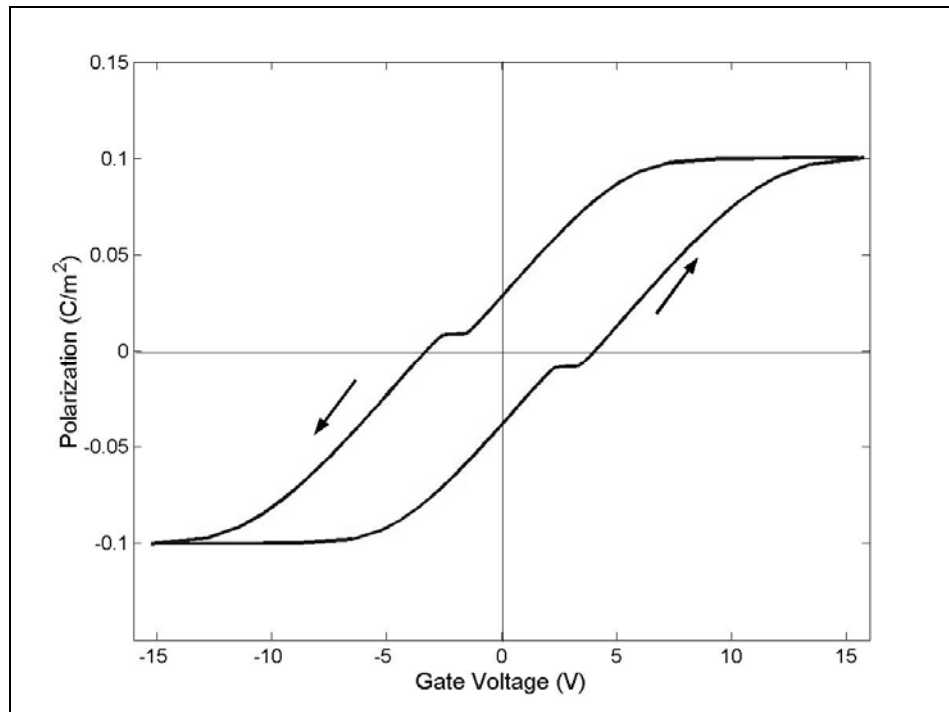


Fig. 3.8 Ferroelectric polarization vs. gate voltage.

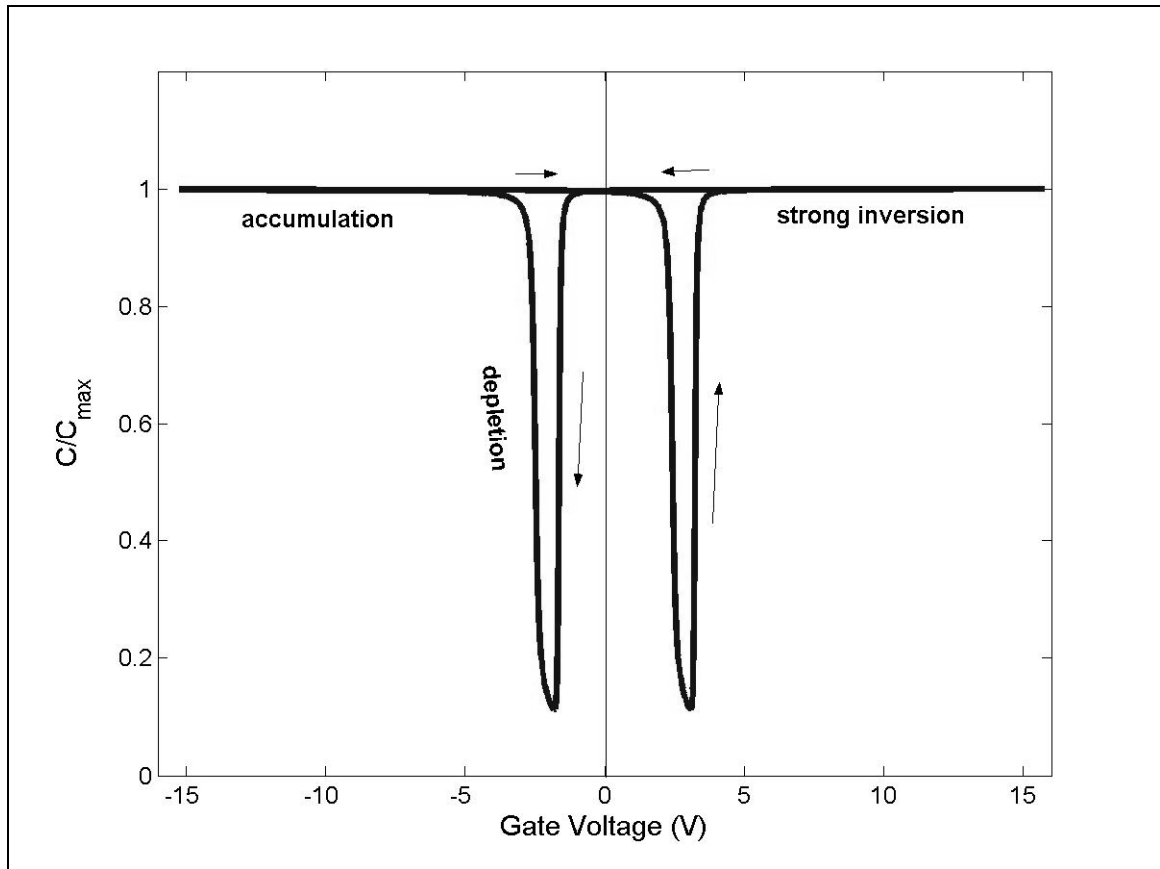


Fig. 3.9 Capacitance Voltage characteristics of modeled MFIS capacitor

**Table 3.1**

Parameter	Value
silicon doping level (p-type)	$1 \times 10^{16} \text{ cm}^{-3}$
dielectric constant of insulator (hafnium oxide)	25
insulator thickness	10 nm
ferroelectric polarization at saturation	$0.1 \text{ C/m}^2$
coercive field	125 MV/m
ferroelectric thickness	20 nm
dielectric constant of ferroelectric	10

## CURRENT STATUS OF METAL-FERROELECTRIC-INSULATOR-SEMICONDUCTOR (MFIS) STRUCTURES

Nonvolatile memories are of great importance in information technology. Memory types within this category include Flash and EEPROM (electrically erasable programmable read only memory), both based on the floating gate transistor; MRAM (magnetic random access memory), FRAM (ferroelectric random access memory) and lastly the FeFET based memory (see table 4.1 for a comparison). Currently, the market is dominated by the Flash type memory, due to its very high memory density and low cost. Therefore, a brief description of the floating gate transistor will be given here.

### 4.1 THE FLOATING GATE TRANSISTOR

The floating gate transistor is essentially a metal-oxide-semiconductor field effect transistor (MOSFET) with an additional gate metal completely embedded within the oxide layer (see fig. 4.1). In order to write information using this structure, the drain is grounded while separate voltages are applied to the control gate and source. The voltage applied to the control gate is much higher, which causes the source electrons to accelerate and these are injected into the floating gate. This write mechanism is called hot channel injection or channel hot electron (CHE).<sup>1</sup> To erase the information, a voltage is applied to the source while grounding the control gate and floating the drain. This causes the electrons in the floating gate to tunnel back to the source. The erase mechanism is Fowler-Nordheim tunneling and it is a slower process than writing.<sup>1</sup>

## 4.2 MFIS STATE RETENTION

In principle, the ferroelectric field effect transistor could be an excellent building block for nonvolatile random access memory since it combines the potentially high speed and low energy consumption of FRAM with the high density of Flash. However, the retention times of these transistors are generally reported at a few days at best, much less than the 10 year requirement for nonvolatile memory. The 2002 paper by T. P. Ma and J. P. Han<sup>2</sup> summarizes the issue and attributes short retention times to two main causes: 1) the depolarization field and 2) the finite leakage current through the dielectric stack.

The depolarization field was already mentioned in the previous chapter. This field is present because the surface charges of the polarized ferroelectric are not fully compensated by the oxide or semiconductor in direct contact with the ferroelectric. The depolarization field is always opposite to the direction of the polarization state and can lead to depolarization of the ferroelectric layer. However, there are claims that the depolarization decay is not too serious under low depolarization field ( $E_{\text{dep}} \ll E_c$ ) to greatly affect the retention characteristics of the MFIS structure.<sup>3</sup>

Possibly the more limiting factor is the gate leakage current and subsequent trapping of charge carriers in the gate dielectric. The ferroelectric polarization can attract charge injection from both the gate metal and semiconductor side of the device. Electron injection is then followed by charge trapping in the dielectric stack which can lead to local charge compensation, but this diminishes the effect of the ferroelectric polarization on the silicon surface charge.

The expected leakage time  $t$  for a device that has a remanent polarization  $P_r$ , leakage current  $I$  and trapping probability  $\alpha$ , may be estimated by:<sup>2</sup>

$$t = \frac{P_r}{I\alpha} \quad (4.1)$$

For typical values of device parameters,  $P_r = 5 \frac{\mu C}{cm^2}$  and  $I = 5 \times 10^{-8} \frac{A}{cm^2}$ , the retention time can vary between 100 seconds (for maximum trapping probability,  $\alpha = 1$ ) to 10 days (for very low trapping,  $\alpha = 10^{-4}$ ). Therefore, the target leakage current required for excellent retention times should be much lower ( $I \ll 10^{-10} \frac{A}{cm^2}$  at the operating field). It has been proposed that an additional insulating layer placed between the ferroelectric and gate electrode (MIFIS capacitor) can greatly improve retention characteristics,<sup>3</sup> but this will further increase the depolarization field as well as the operating voltage.

#### 4.3 PEROVSKITE FERROELECTRICS IN MFIS STRUCTURES

In the literature, the investigated perovskite ferroelectric layers within the MFIS structure include lead zirconate titanate PZT ( $Pb(Zr_{0.53},Ti_{0.47})O_3$ ), lanthanum substituted bismuth titanate BLT ( $Bi_{3.25}La_{0.75}Ti_3O_{12}$ ), and strontium bismuth tantalite SBT ( $SrBi_2Ta_2O_9$ ). Table 4.2 summarizes the basic ferroelectric properties of these materials. The quoted values for the remanent polarizations of PZT and SBT cover a large range and it may be that the lowest values of the table are for unsaturated films. Switching within BLT films occur along two different crystal axis. Within the MFIS structure, switching along the c axis is preferred because it provides sufficient polarization at lower coercive fields. It seems that BLT is receiving the most attention lately because of its enhanced nonfatigue behavior that is comparable to SBT and superior to that of PZT<sup>10</sup> and its better stability at high temperature.<sup>11</sup> The insulating layers that have been studied include  $SiO_2$ ,  $Si_3N_4$ ,  $Al_2O_3$ ,  $ZrO_2$ ,  $TiO_2$ ,  $MgO$ ,  $Y_2O_3$ ,  $HfO_2$ , and  $Dy_2O_3$ .<sup>7</sup>

Table 4.3 lists the memory characteristics of several MFIS structures based on perovskite ferroelectrics. Operating voltages range from 5-15 Volts and at least 3 of the structures show that the measured memory windows have values that are close to the theoretical values for their films ( $\Delta V = 2E_c d_F$ ). The measured value of the memory window will diverge from the expected value depending on how well the ferroelectric polarization is saturated and the amount of injected charge. However, due to the wide range of reported parameters (see Table 4.2), it is difficult to verify whether or not the reported theoretical values are based on coercive fields for fully saturated films.

Table 4.4 lists the memory retention times for some of the same MFIS structures included in Table 4.3. The table includes information on the pulses that were used to ‘write’ the film into its two polarization states. The highest retention times occur at gate voltages where the on/off ratio for capacitance is at a maximum. Often this occurs at nonzero voltage due to finite trapped charge within the insulator and so many of the retention studies are performed at a holding voltage (5<sup>th</sup> column of Table 4.4). Those studies are less impressive because they do not represent a truly nonvolatile memory element. The final column of the table describes the reduction in the capacitance difference between the two states after the time duration given in the first column. All of the structures listed have significant falloff in capacitance on/off ratio within a couple of weeks. It should be noted that the report for the structure that includes the MgO buffer layer extrapolated the data by assuming that the degradation rate does not vary with time and found that the structure will still maintain a significant on/off ratio even after 10 years, an impressive feat (Fig. 4.2), although the 3 V holding voltage will need to be applied that long too. By inspecting both Table 4.3 and 4.4, it is clear that the structures with the best retention characteristics also tend to have the lowest current densities. Therefore, it would be



advantageous to discuss a few of the more recent developments that have reduced leakage within the MFIS structure.

In 2002, C. L. Sun et al.<sup>16</sup> revealed that the performance of MFIS structures based on BLT films formed on  $\text{Al}_2\text{O}_3$  buffered silicon was greatly affected by the annealing temperature. Fig 4.3 shows scanning electron microscopy (SEM) images taken at three different annealing temperatures. It is clear from the images that as the anneal temperature increased, the grain sizes of the BLT films increased significantly. Capacitance-voltage curves recorded from the samples also showed improvement in the size of the memory window. The largest window (13 V) was observed for the sample annealed at  $950^\circ\text{C}$ , while the window for the sample annealed at the lowest temperature ( $700^\circ\text{C}$ ) was actually counterclockwise instead of the usual clockwise orientation expected from a ferroelectric on p type silicon. Fig 4.4 shows that the annealing temperature also had a dramatic affect on the current density characteristics. The improvements may be explained by the reduction of grain boundaries which are believed to be the sources of trapping centers.

Based on the above, a possible solution may arise from the growth of a single crystal, single domain ferroelectric on silicon.<sup>2</sup> In addition to reducing the current density, having a single domain could also reduce the effect of the depolarization field because it affords the possibility of a perfectly “square” hysteresis loop, meaning that fields below the coercive value will not affect the state even over very long periods of time. It seems that significant progress has been made in recent years in growing single crystal ferroelectrics on silicon substrates.<sup>17</sup>

In 2003, T. Y. Tseng et al.<sup>12</sup> reported on the fabrication of MFMIS structures consisting of Pt/BLT (180 nm)/ $\text{LaNiO}_3$  (25 nm)/ $\text{Ba}_{0.7}\text{Sr}_{0.3}\text{TiO}_3$  (16 nm)/Si. By varying the area ratios

between the top gate metal and bottom from 1:1 to 1:16 (Fig. 4.5), they were able to achieve the longest retention time (>11.6 days) in structures of this nature. It is not clear if the impressive retention time is due to better charge screening by the floating gate or improved interfaces. The leakage charge density measured for this structure was especially impressive ( $J \approx 1 \times 10^{-10} \frac{A}{cm^2}$ ). The MFMIS structure is particularly convenient because the flexibility in the area ratios between ferroelectric and insulator can assist in the avoidance of breakdown in the insulating layer. However, the floating gate increases the overall cell area and makes high memory density less feasible, which is a key reason for considering the FeFET based memory.

#### 4.4 PVDF COPOLYMERS IN MFIS STRUCTURE

Other than the literature that is associated with the present study,<sup>18-20</sup> there have been few publications involving PVDF copolymer films incorporated within the metal-ferroelectric-insulator-semiconductor structure. The first study occurred in 1986 by N. Yamauchi.<sup>21</sup> This paper is noteworthy because it addressed the problem of breakdown voltage in the buffer layer and limited carrier injection into the ferroelectric by adding an additional buffer layer on top of the ferroelectric. The sample consisted of 80 nm of spin-coated PVDF:TrFe (73:27) on p-si (3-5  $\Omega$ -cm) with a 50 nm grown oxide layer. An additional 72 nm thick SiO<sub>2</sub> was deposited on top of the polymer film by RF magnetron sputtering at a temperature below 200°C as well as an aluminum gate electrode formed by DC sputter deposition and patterned using photolithography. This MIFIS device exhibited a maximum memory window of just under 40 V after 100 V gate application measured with a high frequency (1 Mhz) CV curve.

The paper also reported on the fabrication of a ferroelectric field effect transistor based on the same structure (Fig. 4.6). Since the copolymer film has a relatively low melting temperature, the

source and drain regions were completed before the polymer film was fabricated. The transistor consisted of a 1  $\mu\text{m}$  thick 75:25 copolymer film sandwiched between two  $\text{SiO}_2$  layers (50 and 100 nm) with an Al-Si film used for the gate. The gate was delineated using photolithography, where the insulating regions were removed over the source and drain regions by reactive ion etching. The MIFIS transistor with a channel width of 12  $\mu\text{m}$  and width of 1.5-10  $\mu\text{m}$  showed an impressive on/off ratio in the drain current ( $> 10^6$ ), but required nearly 200 V gate operation.

In 2004, Lim et al.<sup>22</sup> reported on the characteristics of an MFIS capacitor consisting of a 150 nm thick Ti gate electrode, 450 nm 80:20 PVDF:TrFe film formed by spincoating on n-Si (1  $\Omega\text{-cm}$ ) with an 80 nm oxide layer. The presence of the thick, high bandgap buffer layer, resulted in impressive low leakage currents ( $< 10^{-9}$  A/cm<sup>2</sup> during a 30 V sweep). Investigation of 40 Volt P-V curves for MFM films revealed remanent polarization and coercive voltage values of  $\sim 6 \frac{\mu\text{C}}{\text{cm}^2}$  and 20 V respectively. The maximum polarization achieved in the MFIS structure was  $2 \frac{\mu\text{C}}{\text{cm}^2}$  with a 60 V gate application. This device exhibited a ferroelectric memory window in the high frequency (400 khz) C-V curve of 13.3 V after a  $\pm 30$  V gate sweep. By investigating the flatband shift from the ideal curve of the MFIS and corresponding MIS capacitors, the authors were able to estimate the effective trapped charge densities of -  $1.2 \times 10^{10} \text{ cm}^{-2}$  and  $+9.3 \times 10^{11} \text{ cm}^{-2}$ , indicating that fixed charges bound to the copolymer were negative and strong enough to overcome the effect of fixed positive charges present at the silicon surface. The internal field caused by positive bound charges within the  $\text{SiO}_2$  buffer layer and negative bound charges in the polymer affected polarization switching through partial pinning of the ferroelectric dipoles, resulting in an asymmetric memory window.

In 2005, Gelinck *et al.*<sup>23</sup> presented a potentially low cost nonvolatile technology by reporting on the characteristics of an all polymer thin film transistor based on a 150-550 nm thick spin-coated PVDF copolymer film (Fig. 4.7). In this case, the copolymer is a natural choice for the ferroelectric layer since the low annealing temperature is compatible with flexible plastic substrates. They demonstrated an on/off ratio of  $10^3$  in drain current for channel dimensions of 5 and 1000  $\mu\text{m}$ . Retention studies were performed by measuring the remnant drain currents at zero gate voltage after 100 msec. pulses of + and – 15V. It was found that after 1 hour the on/off ratio in drain current deteriorated to 30% of its initial value, likely due to ionic contaminations from the conducting polymer layer.

#### 4.5 DISCUSSION

The FeFET nonvolatile memory type has many attractive qualities, but the retention characteristics must be improved before it can be used as an alternative to Flash technology. Retention in perovskite MFIS devices seems to be closely tied to the current density of the structure as well as the crystallinity of the ferroelectric film. Devices based on copolymers of P(VDF-TrFE) provide different opportunities but also face different challenges than perovskite devices. The copolymer films can be annealed at much lower temperatures and have lower dielectric constants, but their coercive fields can be several orders of magnitude higher than the perovskite ferroelectrics. As the ferroelectric layer of the copolymer is reduced in order to decrease operating voltage, careful attention should be applied to the current density, which may limit retention times.

## References

1. M. Fitsilis, Ph.D., Institut für Festkörperforschung, Jülich, Germany (2005).
2. T. P. Ma and J. P. Han, *IEEE Electron Device Lett.* **23**, 386 (2002).
3. Z. M. Takahashi, H. Sugiyama, T. Nakaiso, K. Kodama, M. Noda, and M. Okuyama, *Jpn. J. Appl. Phys.* **40**, 2923 (2001).
4. B. Tuttle *et al.*, *J. Am. Ceram. Soc.* **76**, 1537 (1993)..
5. T. Haneder *et al.*, *MRS Proceedings Ferroelectric Thin Films IIX* (1999).
6. A. Z. Simões, A. H. M. Gonzalez, C. S. Riccardi, E. C. Souza, F. Moura, M. A. Zaghete, E. Longo and J. A. Varela, *J. Electrocer.* **13**, 65 (2004)..
7. C. Y. Chang, T. P. Juan and J. Y. Lee, *Appl. Phys. Lett.* **88**, 072917 (2006).
8. Y. Fujisaki, T. Kijima and H. Ishiwara, *Appl. Phys. Lett.* **78**, 1285 (2001).
9. S. B. Xiong and S. Sakai, *Appl. Phys. Lett.* **75**, 1613 (1999).
10. Y. Noguchi, M. Miyayama and T. Kudo, *Appl. Phys. Lett.* **77**, 3639 (2000).
11. B. H. Park, B. S. Kang, S. D. Du, T. W. Noh, J. Lee and W. Jo, *Nature (London)* **401**, 682 (1999).
12. T. Y. Tseng and S. Y. Lee, *Appl. Phys. Lett.* **83**, 981 (2003).
13. L. V. Hai, T. Kanashima and M. Okuyama, *Integr. Ferro.* **84**, 179 (2006).
14. T. P. Juan, C. Y. Chang and J. Y. Lee, *IEEE Electron Device Lett.* **27**, 217 (2006).
15. B. E. Park, K. Takahashi, and H. Ishiwara, *Appl. Phys. Lett.* **85**, 4448 (2004).
16. C. L. Sun, S. Y. Chen, S. B. Chen and A. Chin, *Appl. Phys. Lett.* **80**, 1984 (2002).
17. A. Lin, X. Hong, V. Wood, A. A. Verevkin, C. H. Ahn, R. A. McKee, F. J. Walker and E. D. Specht, *Appl. Phys. Lett.* **78**, 2034 (2001).
18. S. Ducharme, T. J. Reece, C. M. Othon and R. K. Rannow, *IEEE Trans. Dev. Mater. Reliab.* **50**, 720 (2005).
19. T. J. Reece, S. Ducharme, A. V. Sorokin, M. Poulsen, *Appl. Phys. Lett.* **82**, 142 (2003).
20. A. Gerber, M. Fitsilis, H. Kohlstedt, R. Waser, T. J. Reece, S. Ducharme, E. Rije, *J. Appl. Phys.* **100**, 124110 (2006).
21. N. Yamauchi, *Jap. J. Appl. Phys.* **25**, 590 (1986).
22. S. H. Lim, A. C. Rastogi, S. B. Desu, *J. Appl. Phys.* **96**, 5673 (2004).
23. G. H. Gelinck, A. W. Marsman, F. J. Touwslager, S. Setayesh, D. M. de Leeuw, R. C. G. Naber and P. W. M. Blom, *Appl. Phys. Lett.* **87**, 092903 (2005).

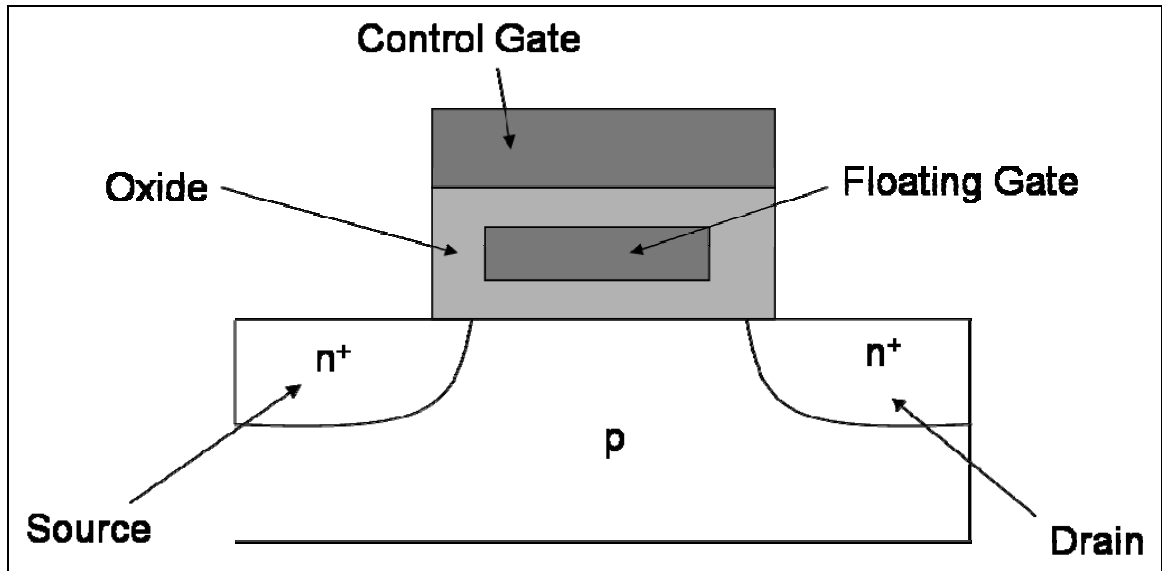


Fig. 4.1 Sketch of the floating gate field effect transistor, the basis for Flash memory.

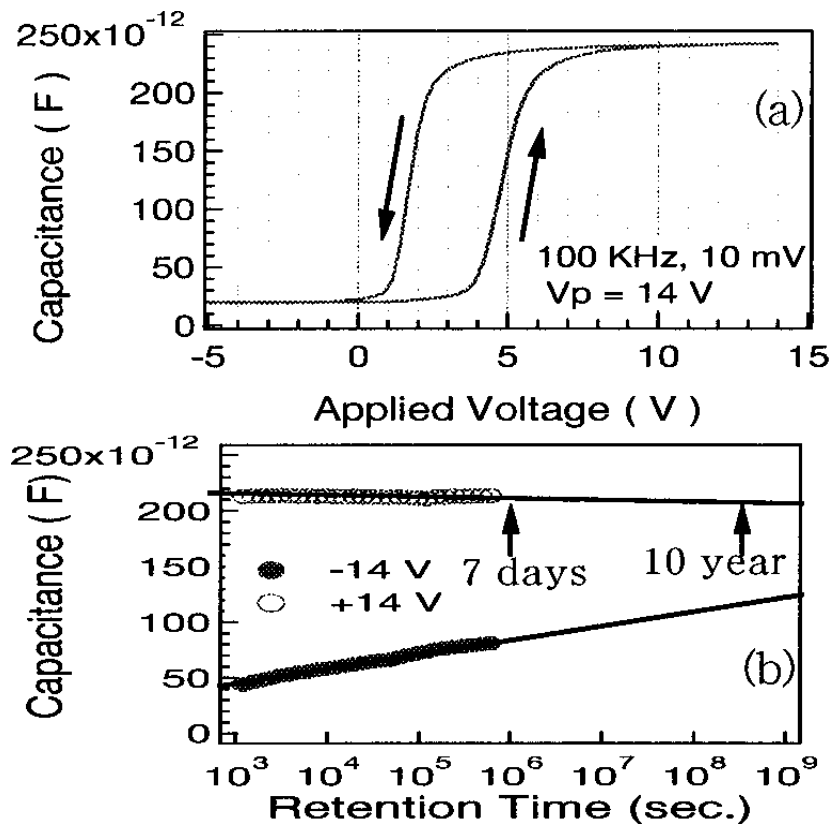


Fig. 4.2 C-V and retention characteristics for Pt/STT/MgO/SiO<sub>2</sub>/Si structure. Reprinted with permission from [9]. Copyright [1999], American Institute of Physics.

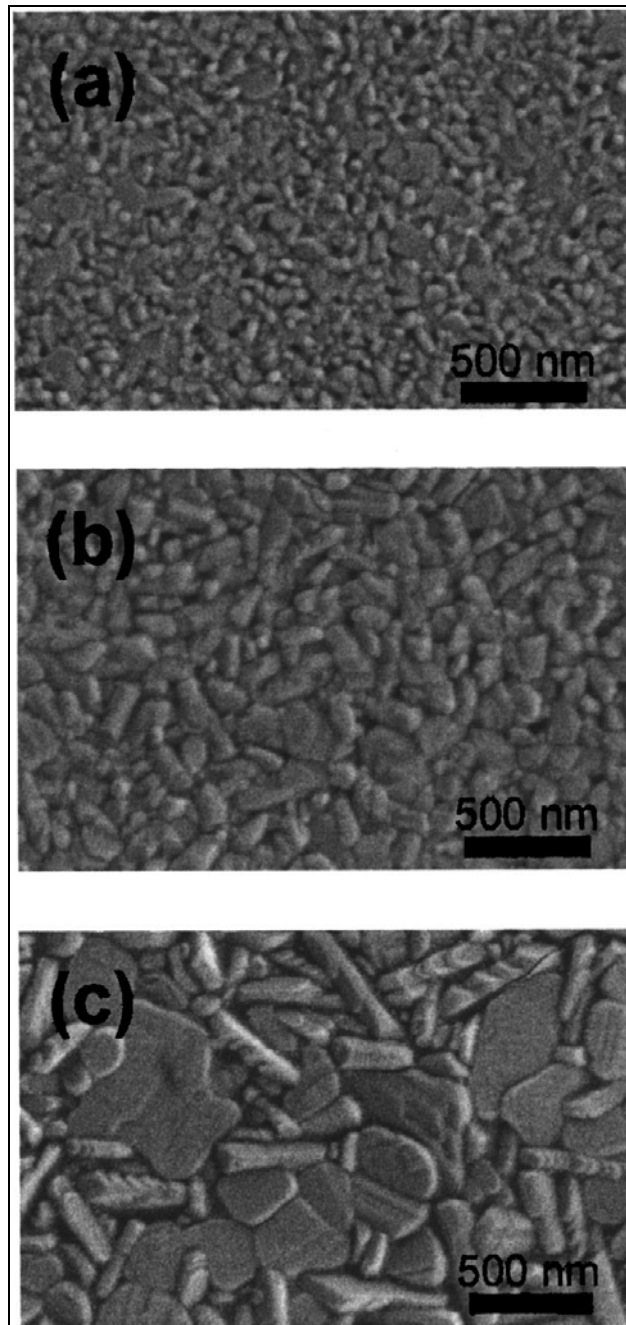


Fig. 4.3 SEM images of BLT film annealed at a) 700°C, b) 850°C and c) 950°C. Reprinted with permission from [16]. Copyright [2002], American Institute of Physics.

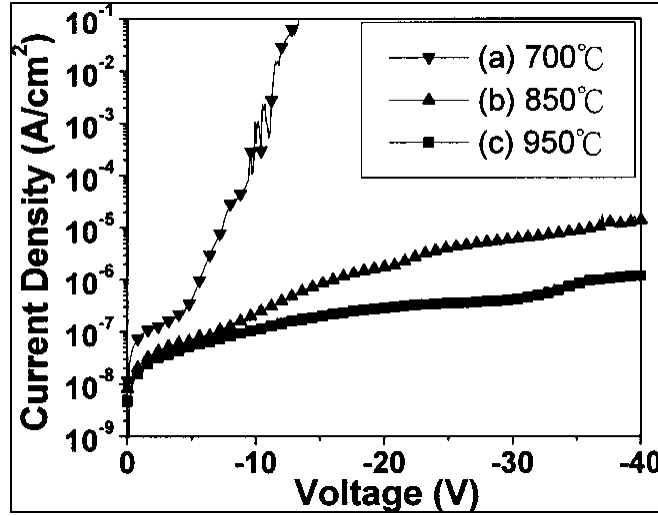


Fig. 4.4 Effect of anneal temperature on current density in BLT films. Reprinted with permission from [16]. Copyright [2002], American Institute of Physics.

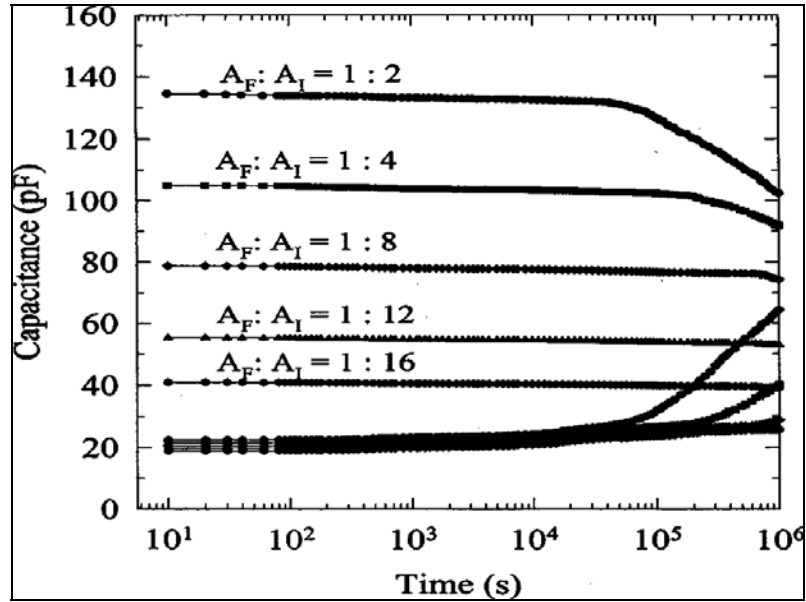


Fig. 4.5 Retention measurements for MFMIS structure including a BLT film for the ferroelectric. The best retention was seen when the area of the buffer layer was 16 times larger than the ferroelectric. Reprinted with permission from [12]. Copyright [2003], American Institute of Physics.



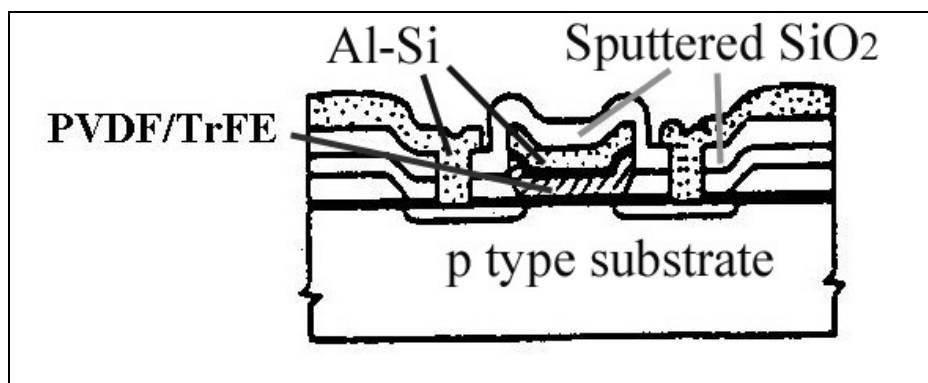


Fig. 4.6 Ferroelectric field effect transistor based on ferroelectric polymer.<sup>21</sup>

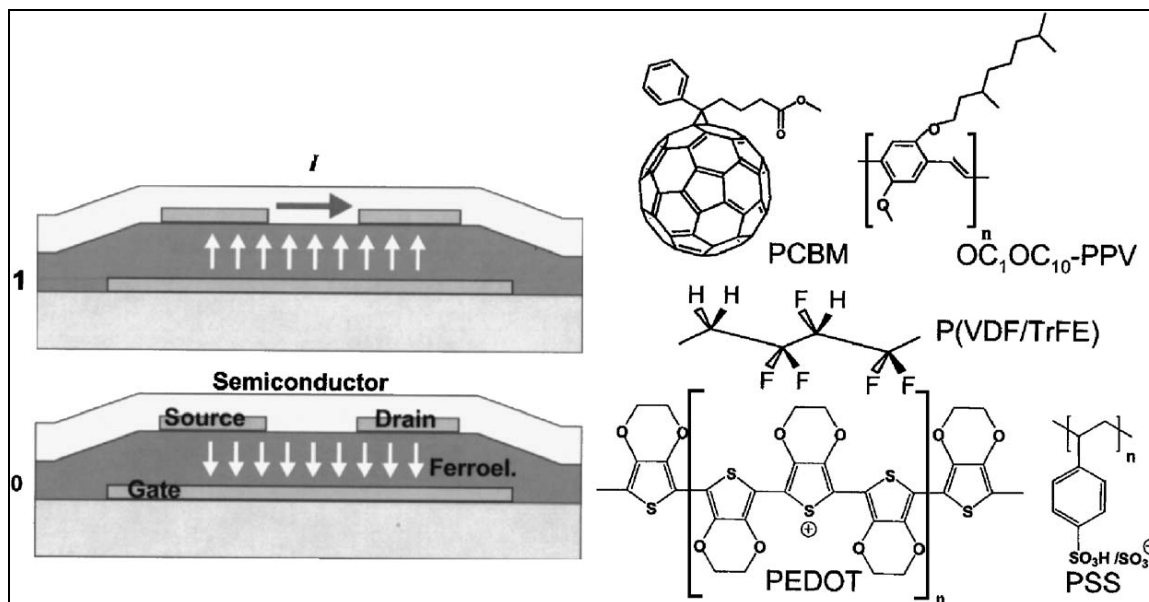


Fig. 4.7 Schematic of an all polymer thin film transistor (TFT) and the chemical structures of the materials used. Reprinted with permission from [23]. Copyright [2005], American Institute of Physics.

**Table 4.1: Properties of nonvolatile memory candidate types.**

Memory Type	Write Access	Read Access	Erase necessary	Destructive Readout	Data Retention	Basic cell
Flash	$\mu\text{s}$	ns	Yes	no	10 years	1T
FRAM	ns	ns	No	yes	10 years	1T-1C
MRAM	ns	ns	No	no	10 years	1T-1MTJ (magnetic tunnel junction)
FeFET	ns	ns	No	no	weeks	1T

**Table 4.2: Basic properties of perovskite ferroelectrics.**

	$P_r$ ( $\mu\text{C}/\text{cm}^2$ )	$E_c$ (MV/m)	$\epsilon_r$
PZT	$3^d$ - $32^a$	$1.6^d$ - $7^a$	$250^a$ - $500^d$
SBT	$3^f$ - $8^b$	$3^b$ - $4^f$	$200$ - $300^f$
BLT	$4$ (c axis) <sup>e</sup> $50$ (a axis)	$0.4^e$ $5$	$160^c$

a) ref. 4

b) ref. 5

c) ref. 6

d) ref. 7

e) ref. 8

f) ref. 9

**Table 4.3: Electrical properties of Perovskite based MFIS structures.**

MFIS structure	Sweep volt. (V)	Window (V)	Theor. Window (V)	Ferro./ins. Thickness (nm)	Current density (C/cm <sup>2</sup> )	Anneal temp. (°C)
Al/PZT/Dy <sub>2</sub> O <sub>3</sub> /Si <sup>g</sup>	10	0.86	0.76	250/20	5- 20×10 <sup>-8</sup>	400
Pt/BLT/Si <sub>3</sub> N <sub>4</sub> /Si <sup>h</sup>	5	1.7	0.1- 0.75	75/3.4	N/A	950
Pt/SBT/MgO/SiO <sub>2</sub> /Si <sup>i</sup>	14	3.1	3.2	400/5/10	N/A	650
Pt/BLT/HfO <sub>2</sub> /Si <sup>j</sup>	7	0.9	N/A	380/N/A	~10 <sup>-9</sup>	750
Au/BLT/Al <sub>2</sub> O <sub>3</sub> /Si <sup>k</sup>	15	13	N/A	N/A/10	~10 <sup>-8</sup>	950
Pt/BLT/LNO/BS T/Si <sup>l</sup>	5	3.1	3.1	180/0.56(EO T)	~10 <sup>-10</sup>	600
Pt/SBT/SiO <sub>2</sub> /Si <sup>m</sup>	6	1.5-2	N/A	400/5.5	~10 <sup>-9</sup>	750

g) ref. 14

h) ref. 8

i) ref. 9

j) ref. 15

k) ref. 16

l) ref. 12

m) ref. 13

**Table 4.4: Retention Properties of perovskite based MFIS structures.**

MFIS structure	Retention time (days)	Ret. Volt. (V)	Write time (sec)	Hold volt. (V)	% drop in $\Delta C$
Pt/BLT/Si <sub>3</sub> N <sub>4</sub> /Si <sup>h</sup>	0.11	5	1	0	5
Pt/SBT/MgO/SiO <sub>2</sub> /Si <sup>i</sup>	7	14	N/A	3	24
Pt/BLT/HfO <sub>2</sub> /Si <sup>j</sup>	5	7	0.1	1.3	32
Pt/BLT/LNO/BS T/Si <sup>l</sup>	11.6	4	1	0	~25
Pt/SBT/SiO <sub>2</sub> /Si <sup>m</sup>	7	6	0.1	0.7	47

FABRICATION AND ANALYSIS OF MFIS STRUCTURES BASED ON  
LANGMUIR-BLODGETT COPOLYMER FILMS

5.1 SAMPLE PREPARATION

Metal-Ferroelectric-Insulator-Semiconductor structures used in this study consisted of a silicon substrate with an insulating layer, a ferroelectric copolymer Langmuir-Blodgett film and an aluminum gate electrode. The ferroelectric layer was deposited in the same manner as layers formed in the metal-ferroelectric-metal cross point arrays described in chapter 2. However in some cases the composition of the copolymer was changed to P(VDF-TrFE) 65:35 (instead of the 70:30 composition used previously). The aluminum top electrodes were made by the same thermal evaporation technique outlined in that same chapter. However the masks used to define the electrode area vary in size, but most of the capacitor structures in this chapter were defined by an electrode area of  $0.24 \text{ cm}^2$ . Electrical contact was made to the back side of the silicon substrates through the formation of an ohmic contact. Establishing a good ohmic contact is not trivial, particularly when the doping level of the silicon is moderate, but good results were achieved when the unpolished side of the wafer was first scratched using a diamond tip glass cutter and a drop of gallium-indium eutectic<sup>1</sup> was painted on the scratch using a toothpick. The whole substrate was then pressed on a flat piece of copper. This method was particularly useful because high temperature treatment was not necessary and the contact can be formed after the LB layer has been deposited. Once the structures were fabricated, the samples were annealed at  $120^\circ\text{C}$  for at least one hour in order to improve crystallinity.

## 5.2 EFFECTIVE TRAPPED CHARGE

Initial studies were made using relatively highly doped ( $< 1 \text{ ohm-cm}$ ) n-type silicon with 100 nm thick  $\text{SiO}_2$  layers from the Polishing Corporation of America (PCA). Fig 5.1 shows capacitance-voltage data for several metal-ferroelectric-insulator-structures, each having a ferroelectric layer with a different thickness. The '0 ML' curve refers to a sample that does not include a ferroelectric layer and therefore is a MOS capacitor. The voltages applied to the MFIS structures were kept low enough to avoid significant hysteresis in the C-V data. The data originates from capacitors made from pieces of the same silicon wafer and the area of the gate electrode was the same for each:  $A=0.24 \text{ cm}^2$ . Unless stated otherwise, all capacitance measurements were made using an impedance analyzer (HP 4192A) with a small test signal of 0.1 V oscillation level at 1 kHz frequency. The gate voltage was ramped using 0.1 V steps at a rate of 0.05 V/sec. Generally, two cycles were performed in order to test repeatability of the data.

Equations 3.16 and 3.34 from chapter 3 were used to estimate the effective trapped charge in each of the structures and the results are summarized in Table 5.1. Since the metal-semiconductor work function difference between the aluminum gate and the silicon wafer is not significantly large, ( $\Phi_{MS} \approx -0.35\text{V}$ ); the flatband voltages for all of the structures are shifted from the ideal curve by a significant negative value. This indicates a large amount of positive trapped charge fixed within the insulating layers, most likely caused by dangling covalent bonds at the silicon surface. By comparing the calculated values for the effective trapped charge within the MFIS structures with that of the MOS capacitor (0 ML), the copolymer seems to contribute negative fixed charges (although this is not true in the 50 ML

case), but the overall effective fixed charge is still significantly positive. The negative contribution agrees with previous reported values in the literature.<sup>2</sup>

### 5.3 CAPACITANCE-VOLTAGE CHARACTERISTICS

At higher applied gate voltages, the MFIS structures show a memory window, since both of the polarization states of the ferroelectric cause the threshold voltage to shift. Fig. 5.2 shows the small signal capacitance data for a 100 ML LB 70:30 film (DMSO solvent) for a gate voltage amplitude of  $\pm 35\text{V}$  (the plot focuses on the region where the depletion layer thickness changes). The minority carrier response is too slow for the 1 kHz frequency of the small signal, so the capacitance remains at the minimum value in the strong inversion mode. After a large positive gate is applied, the ferroelectric is in a polarization state that induces majority carrier charge at the silicon interface. Thus this state favors the accumulation mode and a larger negative voltage is required to reach threshold  $V_{th}$ , the voltage at which the depletion layer reaches maximum thickness and the device capacitance is at a minimum. Conversely, when the large negative gate voltage is applied to the sample, the ferroelectric polarization is switched to the state that induces minority carrier charge at the interface (inversion), and threshold occurs at a smaller negative charge. The counterclockwise orientation of the hysteresis in the figure is therefore consistent with ferroelectric switching. Furthermore, the hysteresis was seen to disappear when the sample temperature was raised to the ferroelectric-paraelectric phase transition.

The size of the memory window was determined by taking the derivative of the data and measuring the voltage separation between intersection points in the slope. In this case, the measured value of the threshold shift was 4.2 V. Based on the threshold voltages

$V_C \geq 10.5V$  for 100 ML MFM samples reported in chapter 2, this value is significantly lower than the expected saturated value of the memory window  $\Delta V_{TH} = 2V_C$  or 21 V. This suggests that significantly larger applied gate voltage is required to fully saturate the ferroelectric, which was also determined in section D of the third chapter (operation voltage). Fig 5.3 indicates that the ferroelectric is not near saturation since it shows that the memory window seems to increase linearly rather than approach a saturation value as the gate voltage amplitude is increased from 15 to 35 V. It should be noted that charge injection from the silicon side into the insulating layers can reduce the size of the memory window.

Fig. 5.4 shows the positions of the threshold voltages that were used to determine the window sizes given in the Fig. 5.3 plot. Since the slopes of the two lines are nearly identical, there does not seem to be evidence for significant charge injection. Since the silicon oxide bandgap presents a larger barrier for holes than electrons, charge injection would be larger after a large positive gate voltage application and this would cause the red data to have a significantly larger slope and lose its linearity. The red data does in fact have a larger slope, but the difference is slight and may be explained by the negative shift in flatband from the ideal curve discussed in section 5.2. Due to the presence of the fixed charge in the oxide and the depletion layer, symmetric gate voltage applications are not equivalent to symmetric field applications across the ferroelectric layer, a slightly lower negative field is applied to the polymer.

#### 5.4 STATE RETENTION

The device capacitance data of the previous section demonstrated that the two bipolar polarization states of the ferroelectric produced a dramatic effect on the surface potential of the n-type semiconductor. However, the stability of those states has not yet been addressed.

The method for investigating device state retention in 100 ML MFIS devices was accomplished in the following matter: First, a +35 V DC gate voltage was applied to across the MFIS. Since it has been established that this voltage pulse is not large enough to saturate the ferroelectric polarization, the bias was applied for 15 seconds in order to increase the remanent polarization. Then, after this voltage was removed, the capacitance was monitored over time for approximately an hour using the HP impedance analyzer. Then the process was repeated with a -35V pulse that was also applied for 15 seconds. For truly nonvolatile memory, retention studies should be made at zero gate voltage. However, since the large effective trapped charge in the insulator led to a negligible on/off ratio in capacitance at zero voltage, the capacitances were monitored at different holding voltages.

Fig. 5.5 reveals the retention data for a 100 ML film (approximately 170 nm) on a 100 nm SiO<sub>2</sub> insulating layer for different values of the holding voltage. The holding voltages were -3 V for the top plot, -6 V for the middle, and -9 V for the bottom figure. In the figure, the higher capacitance (accumulation) state is referred to as the ‘OFF’ state, because within the FeFET structure, this state would induce higher resistance in the channel than the lower capacitance (inversion) ‘ON’ state would. In the case of the -3 V holding voltage, the states quickly converge at the accumulation capacitance. This occurs because -3V is to the right of the flatband voltage and thus the external field across the ferroelectric is positive, which maintains the ‘OFF’ state and switches the ‘ON’ state over time. The opposite situation occurs at the -9 V holding voltages. Both states quickly revert to the ‘ON’ state in this case. Since the -6 V holding voltage is closer to the center of the hysteresis, the two capacitance states are discernible for the longest amount of time at this holding voltage. In this case, the capacitance difference between the two states drops to 56% of its initial value after approximately 1 hour.



The current density ( $J \leq 10^{-8} \frac{A}{cm^2}$  even at high gate voltage) through the MFIS structure (Fig. 5.6) is comparable to the MFIS structures based on perovskite ferroelectrics. Using the value for the current density at 10 V gate bias and assuming that the remanent polarization in the film is low ( $P_r \approx 1 \frac{\mu C}{cm^2}$ ), expression (4.1) from chapter 4 yields estimated retention times of 500 seconds for the highest possible probability of trapping, to over 50 days for very low trapping probability ( $\sim 10^{-4}$ ). The measured retention is closer to the former, which suggests that either the remanent polarization is considerably lower, or the copolymer film has a high probability of trapping injected charge (or both).

## 5.5 PYROELECTRIC MEASUREMENTS

In chapter 2, it was shown that the Chenoweth technique is useful for measuring pyroelectric signals through laser-induced thermal modulation. This method was employed to probe the polarization state of the MFIS capacitor. The measurement was carried out in much the same manner as it was for MFM samples in chapter 2. The films were heated by a 5 mW He-Ne laser chopped at 2 khz. A constant gate voltage was applied to the MFIS capacitor for 30 seconds. The gate bias was then removed and the pyroelectric signal of the sample was recorded after another 30 seconds by the lock-in amplifier referenced to the chopper frequency.

Fig. 5.7 shows the pyroelectric signal and phase for a 35 V sweep (with 5 V steps) of the 100 ML MFIS capacitor. After, positive gate voltage, the remanent pyroelectric signal is quite low, only a few tens of picoamps. This signal is at least an order of magnitude less than the currents routinely measured in MFM samples, suggesting that the polarization is not saturated. The

signal after negative gate voltage applications is surprisingly much larger. However, when the signals were monitored over time, it became clear that the negative pyroelectric state is short-lived. The negative signal switched to the same signal as the positive state within an hour, about the same amount of time as the top plot in the capacitance retention figure. It may be that the transient current involved in the gradual switching of the ferroelectric introduces too much noise at the lock-in frequency to achieve an accurate reading for the actual pyroelectric signal. The piezoelectric technique may be more appropriate for this measurement because since phase deflection of beam used to measure the piezoelectric coefficient is independent of the current flowing through the sample. However, at this time an appreciable piezoelectric signal has not yet been measured in the LB MFIS samples.

## 5.6 SAWYER TOWER MEASUREMENTS

The 100 ML MFIS sample was inserted in the Sawyer Tower circuit described in chapter 2. The Sawyer Tower technique permitted the direct measurement of the surface charge of the device and the voltage amplifier provided gate voltage amplitudes that were not reached with the impedance analyzer. Fig. 5.8 shows Sawyer Tower polarization hysteresis loops for the sample achieved from 10 hz triangle waveforms with increasing amplitudes. At this frequency, minority carrier response time is an issue, so the sample was illuminated with a 15 W halogen lamp to ensure that the loops were symmetric. Even though gate voltages as high as 55 V were applied to the MFIS structure, the remanent polarization never exceeded  $P_r = 0.5 \frac{\mu C}{cm^2}$ , more than an order of magnitude less than the expected saturated value.

## 5.7 COPOLYMER MFIS STRUCTURES WITH HIGH DIELECTRIC CONSTANT INSULATORS

Since it is difficult to saturate thick LB films on a thick silicon oxide layer, the next logical step is to reduce the thicknesses of both layers while increasing the dielectric constant of the insulating layer. This should ensure that the operating voltage is reduced while supplying a larger percentage voltage drop across the ferroelectric layer. Moderately doped p-type silicon wafers (1-10  $\Omega$ -cm) with varying thicknesses of high k insulating layers were provided by colleagues at the Institut für Festkörperforschung in Jülich, Germany. The insulating layers included hafnium oxide ( $\epsilon_{ins} \approx 25$ ), dysprosium oxide ( $\epsilon_{ins} \approx 19$ ) and cerium oxide ( $\epsilon_{ins} \approx 26$ ). In general, MFIS structures fabricated under the same conditions as the ‘thick’ structures using these substrates resulted in large capacitance memory windows even at gate voltages lower than 5 V and lower shifts in flatband voltages due to reduced effective trapped charge in the insulating layer. However, the current densities measured through these capacitors were considerably higher ( $>10^{-6}$  A/cm<sup>2</sup>) and although the voltages needed to saturate these configurations were greatly reduced, these voltages could not be reached without causing dielectric breakdown and significant charge injection.

Fig. 5.9 shows the 2 cycles of a C-V plot for a 15 ML 65:35 LB film deposited on 30 nm of cerium oxide. The ferroelectric layer now causes hysteresis that has a clockwise orientation since the substrate is now p type. The gate amplitude for the data was only 5 V, yet the threshold shift was already 1.1 V. This value is nearly 1/3 of the expected value of 3.9 V based on data from the capacitance measurements shown in chapter 2 for a 15 ML MFM capacitor. However, Fig. 5.10 shows that when the gate amplitude was increased, the window achieved its maximum value of 1.9 V (more than half of the theoretical saturated value) at a gate amplitude of 7 V and then the size of the window begins to decrease. Furthermore, both of

the threshold voltages show a trend of shifting to more positive (or less negative) values, an indication that negative charge is being injected from the silicon side.

The stability of the polarization states was monitored in the manner described in section 5.4. Since the on/off ratio was significant at zero bias, in this case the capacitance was monitored over time without a holding voltage. Fig. 5.11 shows the ‘OFF’ or accumulation capacitance state and its dependence with time after two -6 V pulses with varying time durations. The process was also performed with the ‘ON’ state, but for simplicity that data is not shown since the stable ‘ON’ state varied little with time. Although the large window of the capacitance loop indicates that the ferroelectric film was brought closer to saturation when compared to the earlier studies on thick MFIS structures, there is little (if any) improvement in the retention data. It is likely that the higher current density plays a prominent role in the limited retention characteristics for thin LB copolymer films on insulators with high dielectric constants.

In conclusion, the device characteristics of MFIS structures involving thick LB copolymer films on thick silicon oxide were investigated. The results of several experimental methods indicated that the polarization of the ferroelectric was not saturated, even though gate voltages as high as 55 V were applied. The current densities measured through these structures were comparable to those measured in MFIS structures based on perovskite ferroelectrics. However, the limited retention time of the copolymer based devices suggested that the trapping probability is higher. To improve performance, it may be necessary to thoroughly investigate the effect of growth conditions on the amount of crystallinity in LB films.

In order to reduce operating voltages and to better saturate the ferroelectric, much thinner LB films were deposited on silicon substrates that had thin buffer layers with high dielectric

constants. These structures resulted in repeatable hysteresis at lower voltages and better on/off ratios at zero bias, which is necessary for a nonvolatile memory. However, improved retention properties were not evident because larger leakage currents were produced in these configurations. In order to decrease operating voltages and maintain acceptable current densities, it may be necessary to grow a second high  $k$  buffer layer between the ferroelectric and gate metal while investigating methods to improve overall crystallinity in the LB polymer films.

## References

1. Y. Tokuda and T. Seki, *Semicond. Sci. Technol.* **15**, 126 (2000).
2. S. H. Lim, A. C. Rastogi, S. B. Desu, *J. Appl. Phys.* **96**, 5673 (2004).

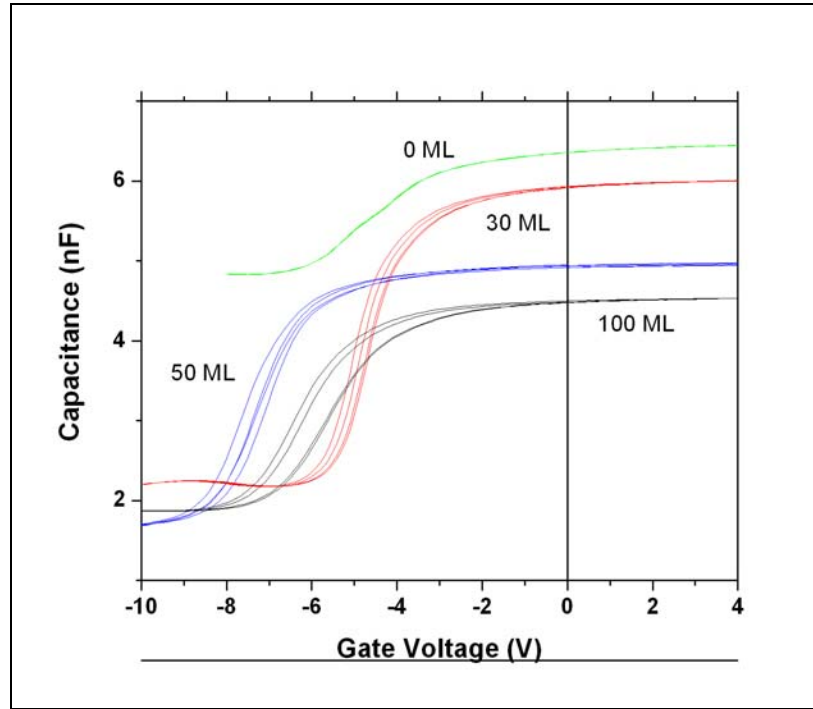


Fig. 5.1 Capacitance-Voltage loops for MFIS structures with a 100 nm SiO<sub>2</sub> insulating layer and ferroelectric copolymer films of varying thicknesses.

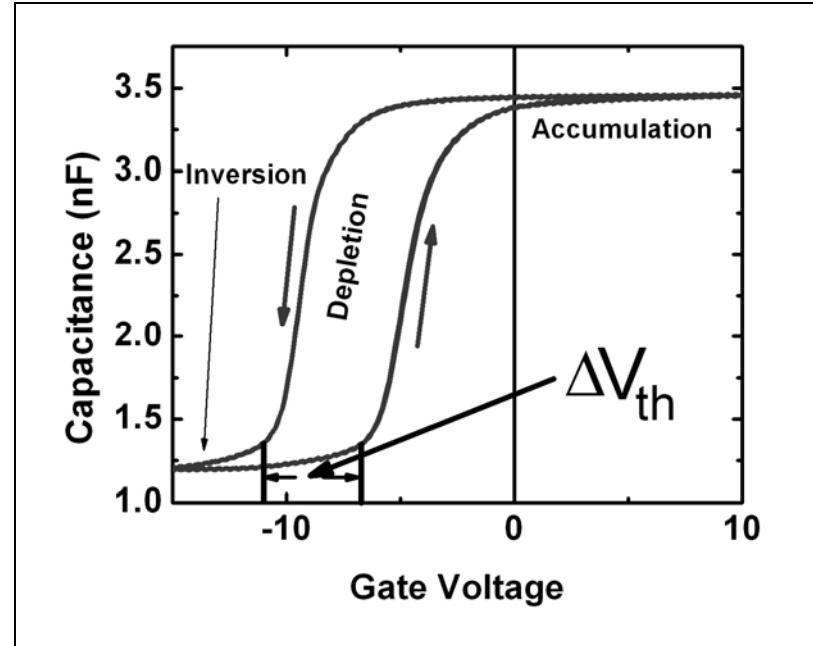


Fig. 5.2 Capacitance Voltage data for 100 ML MFIS structure showing a large shift in the threshold voltage. The amplitude of the gate voltage was 35 V.

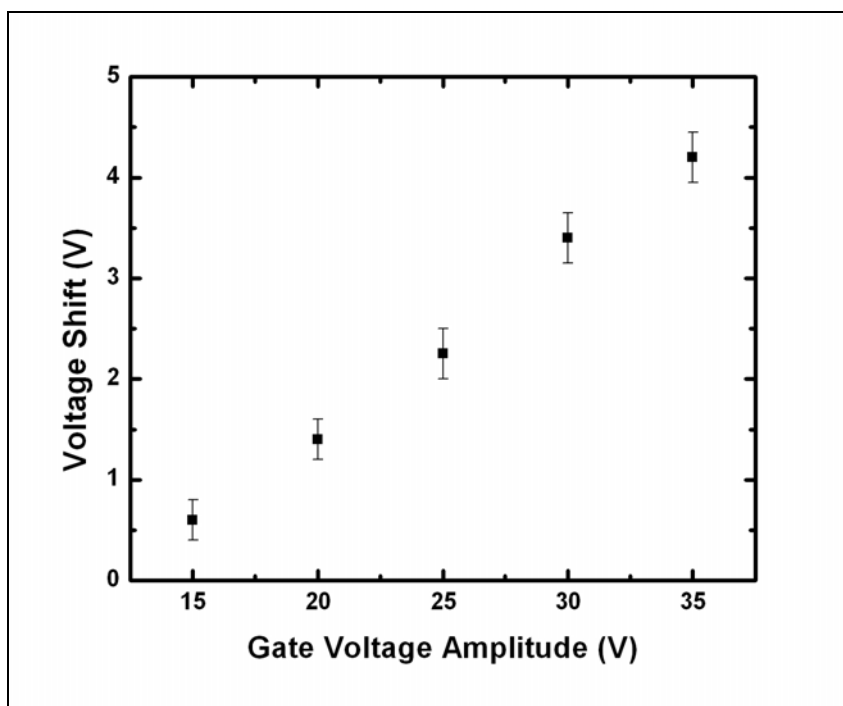


Fig. 5.3 Dependence of memory window size on gate voltage amplitude for a 100 ML MFIS.

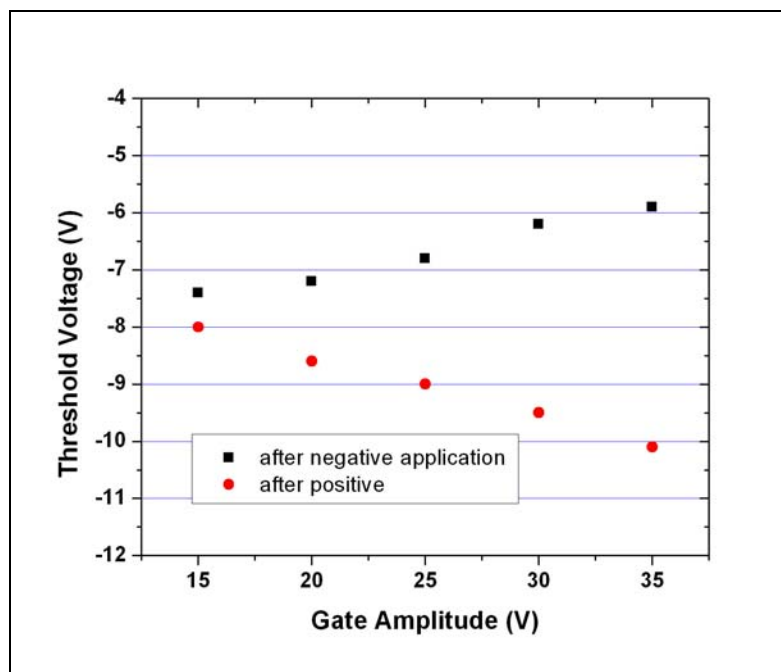


Fig. 5.4 Positions of the two threshold voltages for different values of the applied gate amplitude.



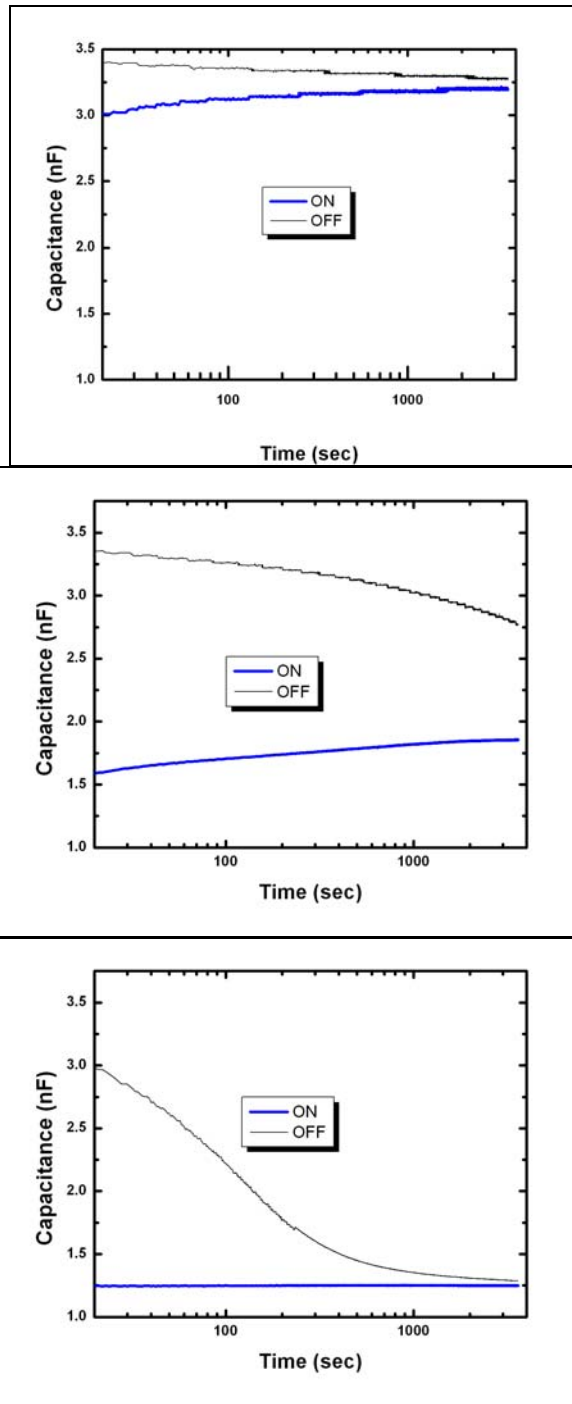


Fig. 5.5 Capacitance retention measurements at holding voltages of -3V (top), -6V (middle) and -9V (bottom)

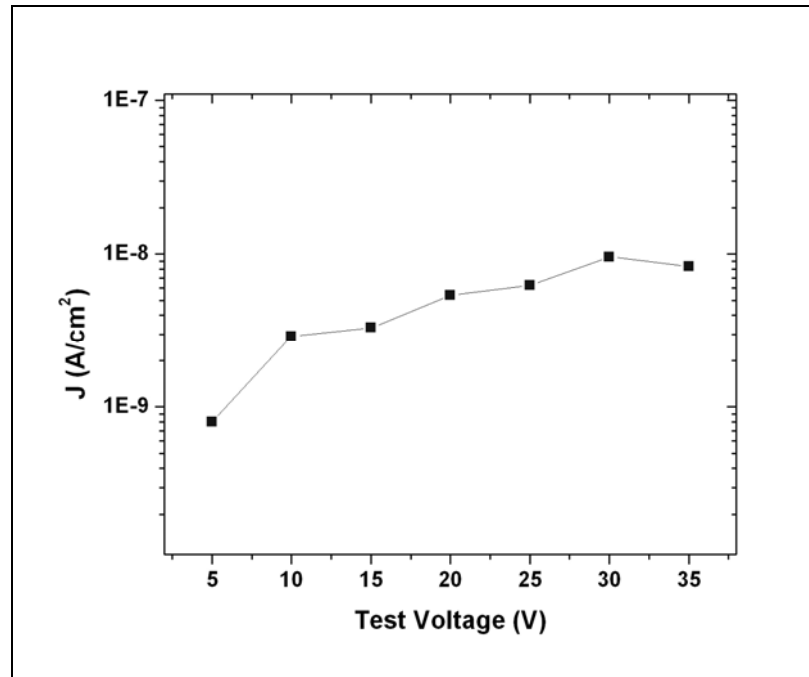


Fig. 5.6 Current density characteristics through a 100 ML MFIS capacitor.

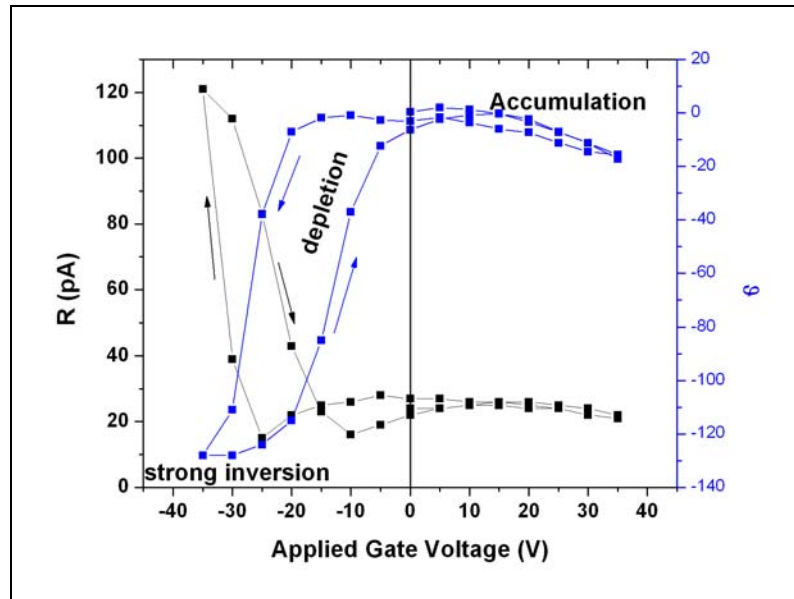


Fig. 5.7 Pyroelectric signal and phase for a gate voltage sweep of a 100 ML MFIS capacitor.

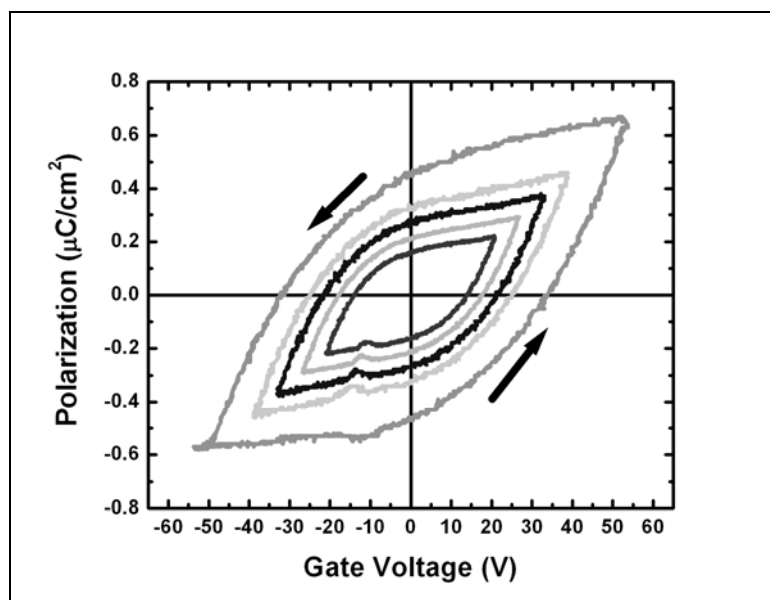


Fig. 5.8 Sawyer Tower loops at increasing amplitudes from a 100 ML MFIS sample.

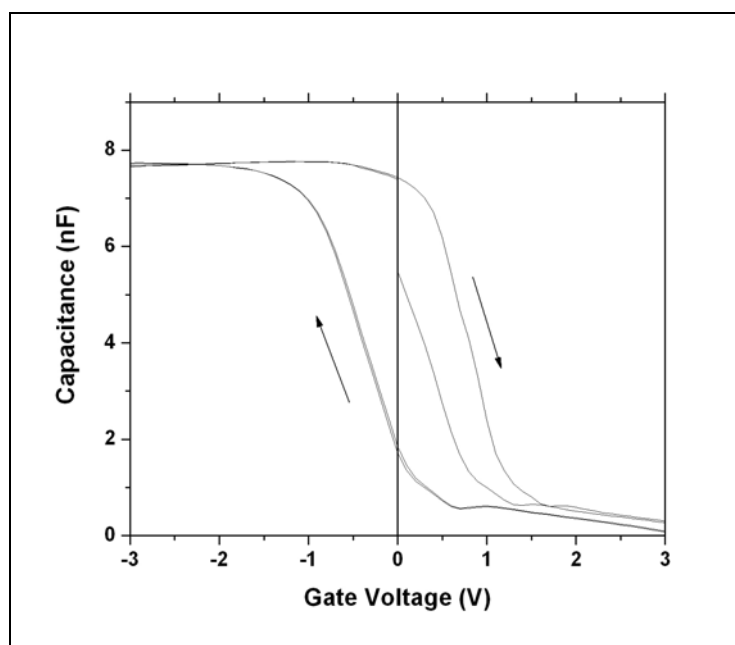


Fig. 5.9 C-V loop for a 15 ML 65:35 LB film on 30 nm cerium oxide layer.

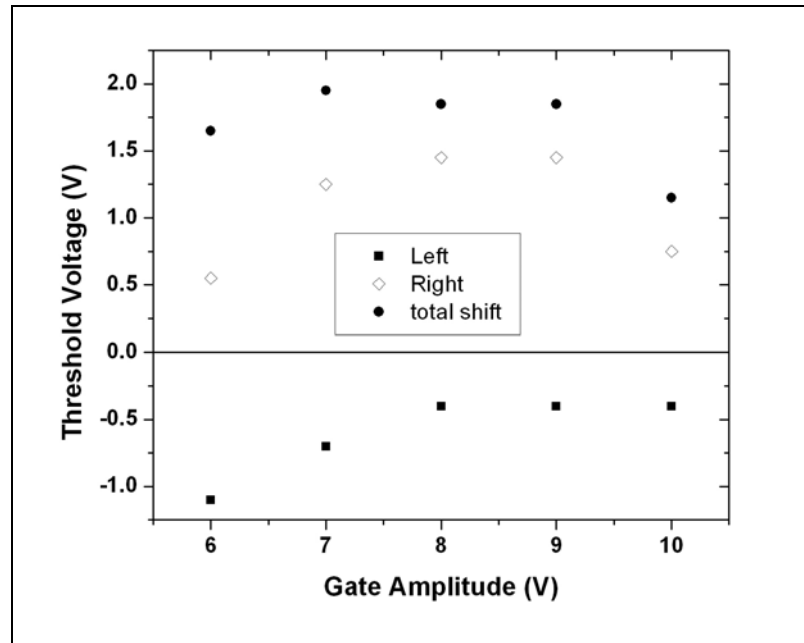


Fig. 5.10 Threshold voltages and memory window for the 15 ML LB film on 30 nm cerium oxide.

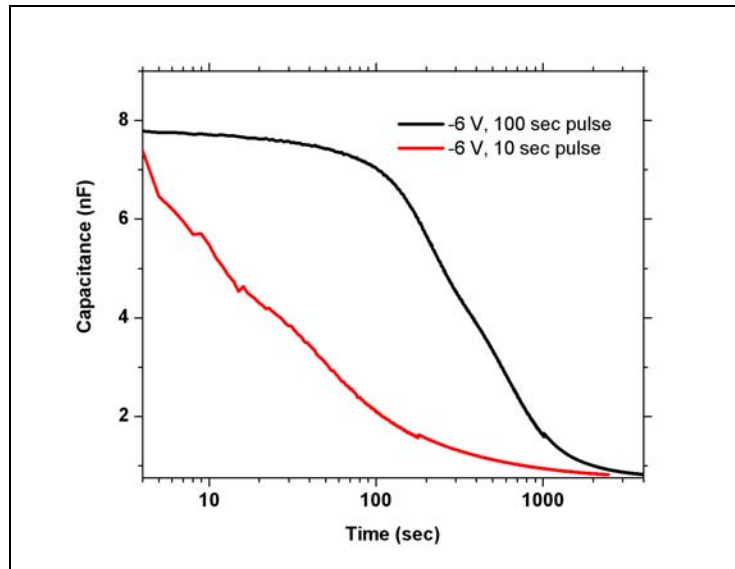


Fig. 5.11 retention of the accumulation state of the MFIS structure with 15 ML 65:35 on 30 nm cerium oxide.

# Table 5.1

Number of LB deposition steps	$C_{acc}$ (nF)	$C_{FB}$ (nF)	Flatband Voltage (V)	eff. $Q_{trapped}$ ( $\mu C/cm^2$ )	net $Q_{trapped}$ ( $\mu C/cm^2$ )	eff.
0	6.36	5.78	-4.0	+0.100		
30	5.93	5.42	-3.5	+0.080	-0.020	
50	4.96	4.6	-5.5	+0.110	+0.010	
100	4.49	4.19	-4.1	+0.077	-0.023	